A 65nm CMOS Wideband TDD Front-End with Integrated T/R Switching via PA Re-Use

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***Abstract*—A wideband time-division duplex (TDD) front-end with an integrated transmit/receive (T/R) switching technique is implemented in 65nm CMOS. By re-using the PA as an LNA during receive mode, the system eliminates the conventional series T/R switch from the signal path and utilizes only DC mode control switches to enable TDD co-existence. With integrated front-end balun transformer, the full polar transmitter achieves 20dBm peak output power with 32.7% peak drain efficiency. In receive mode, the PA is reconfigured into a wideband 3.4GHz-5.4GHz LNA achieving -6.7dBm P1dB and 5.1dB NF.**

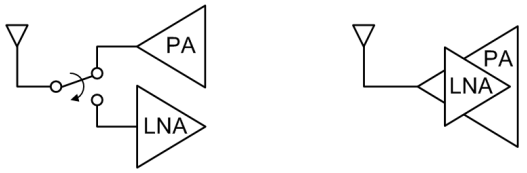
I. Introduction

Time-division duplex (TDD) co-existence with high transmit power is conventionally enabled by discrete T/R switches (TRSWs), which are off-chip and inherently narrowband. As mobile devices must support increasingly more wireless standards and bands, the number of discrete front-end components needed - including TRSWs - increases accordingly, resulting in greater cost and PCB area. Furthermore, discrete TRSWs are accompanied by additional degradations from PCB and package parasitics. Thus, there is significant interest in integrated wideband TRSWs to support modern multi-band radios.

Due to the PA's high output power and resulting voltage swings beyond those tolerated by modern CMOS devices, integrated TRSWs require floating wells and accurate knowledge of substrate characteristics to ensure robustness [1] [2]. In addition, integrated TRSWs are generally also narrowband, relying on sharp resonance to provide adequate isolation [1] [3], while wideband switches have demonstrated higher losses of 2dB and greater [4] [5].

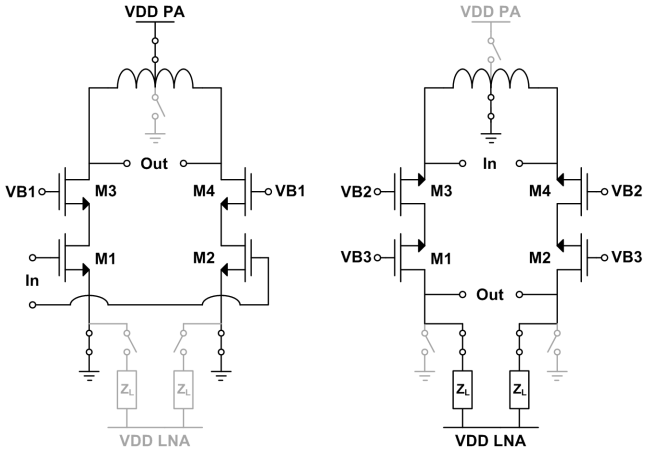
We propose an innovative architecture with integrated T/R switching for wideband TDD co-existence. Instead of using a front-end switch to isolate and select between PA and LNA blocks, the PA is re-used as an LNA during receive mode. Fig. 1 illustrates the proposed scheme. Isolation is no longer an issue as the PA and LNA are the same block, with a single antenna port. The conventional in-line TRSW that contributes significant insertion loss, especially at high frequencies, has been eliminated. Instead, there are only DC power and control switches to enable PA to LNA transformation.

As proof-of-concept for the proposed T/R switching technique, we present a TDD front-end composed of a polar transmitter, a PA re-usable as an LNA, and integrated front-end balun. The system in LNA mode achieves 2.7GHz bandwidth, -6.7dBm P1dB, and 5.1dB NF. In PA mode, the system achieves $P_{SAT} = 20$dBm with 32.7% peak drain efficiency.



(a) (b)

Fig. 1: TDD front-end: (a) conventional, (b) proposed.



(a) (b)

Fig. 2: PA/LNA transformation: (a) PA mode, (b) LNA mode.

II. PA to LNA Transformation

A. Topology

Mixed-signal polar transmitters employing current-switching PAs have demonstrated good power and efficiency performance at gigahertz frequencies [6]. Fig. 2(a) illustrates a typical inverse class-D current-switching PA. Transistors $M_{1,2}$ are the switched PA input devices, and $M_{3,4}$ are cascodes to support high PA output power. This fundamental topology of an input pair plus a cascode pair is identical to a cascoded common-gate LNA, and we exploit this similarity to transform the PA into an LNA.

Fig. 2(b) illustrates the same structure in LNA mode. Supply and ground have been flipped, as have the source and drain of all transistors. Transistors $M_{3,4}$ are now LNA input devices, and their source - formerly their drain and the PA output node - is now the LNA input node. Transistors $M_{1,2}$ are LNA cascodes, and their drain (formerly source in PA mode) is now the LNA output node and connected to an LNA load

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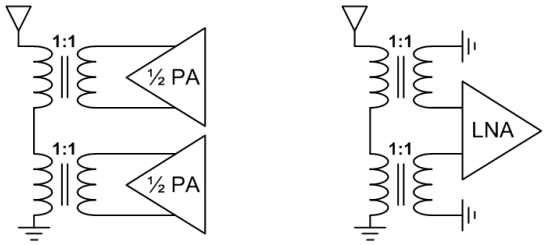


(a) (b)

Fig. 3: Front-end transformer: (a) PA mode, (b) LNA mode.

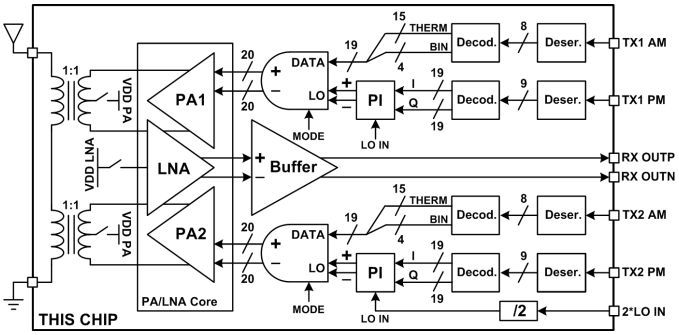


Fig. 4: Block diagram of system top level.

and supply. The PA has thus been transformed into an LNA using only DC power switches.

B. Impedance Co-Match

The PA and LNA's different impedance match requirements are accommodated using transformer-based power combining. This technique has been used to boost PA efficiency in power backoff region by modulating PA load impedance [7], and we utilize that impedance modulation property to provide PA/LNA co-match. Fig. 3(a) shows a transformer power combiner in PA mode. Two identical sub-PAs drive two identical stacked 1:1 sub-transformers. The load impedance seen by each sub-PA is $50\Omega/2 = 25\Omega$, which is sufficiently low.

Fig. 3(b) shows the transformer structure in LNA mode. In contrast to [7], where impedance was reconfigured by shorting a sub-transformer, we place the LNA in between the two sub-transformers. The sub-transformers are in series and act as a single 1:1 transformer with doubled inductance. The 1:1 transformation provides the LNA with a 50Ω match, while the increased inductance lowers tank Q and improves wideband performance. The implemented combined transformer has simulated $L = 1.8$nH and $IL = 1.3$dB.

The ground connections on either side of the LNA become the center tap of the combined transformer. Existing PA devices, which are already large with low on resistance, are used as the switches to ground.

III. System Implementation

The PA re-use TDD front-end is embedded in a full digital polar transmitter as a proof-of-concept. Fig. 4 shows a block diagram of the implemented system. We use the digital transmitter derived from [7], which has an 8-bit amplitude modulator and 9-bit phase modulator. For each sub-PA, identical AM and PM input data are deserialized and decoded. The 8 amplitude bits resolve into 15 thermometer bits and 4 binary bits, each controlling a corresponding PA cell as in a DAC. The decoded phase bits control I/Q current DACs of a Gilbert-cell-based phase interpolator (PI) to generate a differential LO waveform at the desired PA output frequency and phase. The PI's LO output is combined with the amplitude data in an AND operation to create the switching inputs that drive the cells of the PA core. The input LO is routed to the two TX chains driving each sub-PA using a resistive impedance-matched splitter.

In RX mode, the LNA outputs are directly buffered off-chip for measurement. The RX buffer has two common source gain stages followed by a source follower output driver to provide 50Ω. The gain stages exist to minimize the noise contribution of the output driver to system NF, and they are bypassed in LNA linearity measurements.

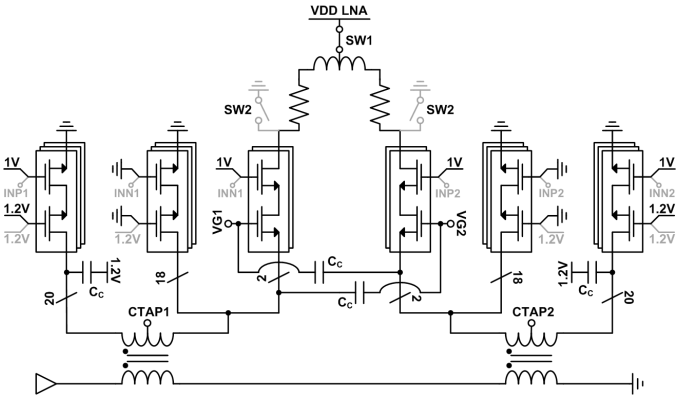
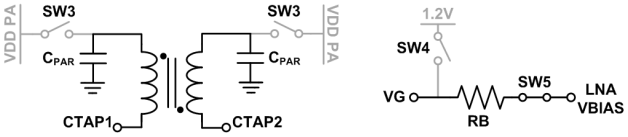


Fig. 5: Schematic of PA/LNA core with front-end transformer. LNA mode is highlighted while PA mode is in gray.



(a) (b)

Fig. 6: Schematic of switches for (a) PA supply, (b) VG bias.

A. PA/LNA Core

Fig. 5 illustrates the PA/LNA core, along with the stacked transformer and both sub-PAs. Each sub-PA has 20 differential PA cells - 15 thermometer cells, 4 binary, and 1 dummy. In PA mode, the top row of transistors are PA input devices, driven by a switching input or turned off depending on amplitude data. The bottom row of devices are PA cascodes, all biased at 1.2V. The sub-transformer center tap nodes $\text{CTAP}_{1,2}$ are connected to PA supply.

The LNA straddles the two sub-transformers and uses 2 thermometer cells per sub-PA. It is a gm-boosted common-gate LNA with a shunt-peaking load. The LNA cascode devices are biased at 1V, the supply voltage of PA input drivers. The cross-coupled capacitors C_C for gm-boosting are absorbed into the front-end tank in both PA and LNA modes, and the side

capacitors are replicated C_C for symmetry during PA mode. The unused PA branches adjacent to the LNA are turned off and act as capacitance at the LNA input. The side PA branches are switched on to create the LNA's input DC connection to ground. The sub-transformer center tap nodes $CTAP_{1,2}$ are disconnected from PA supply and are high impedance.

The LNA uses the 2 highest of the 14 PA thermometer cells in order to have the least effect on PA performance. The highest PA cells would only be turned on when the PA is operating at peak or near-peak power, thus the incorporation of an LNA into the PA core has minimized impact on average PA operation.

B. PA Supply Switch

A schematic of the PA supply switching structure at $CTAP_{1,2}$ is shown in Fig. 6(a). For good PA drain efficiency, the PA supply switches SW3 must be large with extremely low ON resistance. In LNA mode however, SW3's large parasitic capacitance C_{PAR} resonates with the inductance of the front-end transformer and severely degrades LNA performance. To mitigate this effect, we insert a choke inductor between the PA supply switch and $CTAP_{1,2}$, isolating C_{PAR} from the front-end transformer.

As shown in Fig. 6(a), we further inversely couple the two CTAP choke inductors into a transformer. In LNA mode, the two CTAP nodes are differential, and the effective choke inductance at each CTAP is boosted due to transformer coupling. In PA mode, on the other hand, the two CTAP nodes are common mode and their choke inductances cancel. Since a low supply inductance is desirable for the PA, the coupling beneficially impacts both PA and LNA modes. The supply transformer is designed for low resistance to minimize degradations to PA efficiency, and it has simulated $L_{EFF,LNA}$=555pH and $L_{EFF,PA}$=86pH.

C. PA/LNA Mode Switching

Shown in Fig. 5, SW1 and SW2 select between the LNA load and supply for the LNA branches versus PA ground. The LNA supply switch SW1, at the center tap of the LNA's shunt-peaking inductor, is outside of the signal path and has no effect on performance. The PA ground switch SW2, however, occurs at the LNA's sensitive output node and is sized relatively small to minimize loading. The resulting degradation to PA performance is negligible since SW2 exists only in the highest 2 PA thermometer cells.

The LNA's input gate bias $VG_{1,2}$ is set by the structure shown in Fig. 6(b). In PA mode, the LNA's input devices are PA cascodes, and their gates are pulled up to 1.2V by SW4. In LNA mode, VG is biased through SW5 and a large resistor RB to allow voltage swing from gm-boosting.

Finally, all remaining PA/LNA mode-switching is implemented through digital logic. PA cascode devices either remain at their 1.2V cascode voltage or are driven to ground depending on function in LNA mode. Logic is inserted into drivers for the PA input devices to output steady ground or VDD in LNA mode, or to pass the switching LO waveform in PA mode. System control logic times each mode-switching event to prevent the existence of supply-to-ground short circuit at any time.

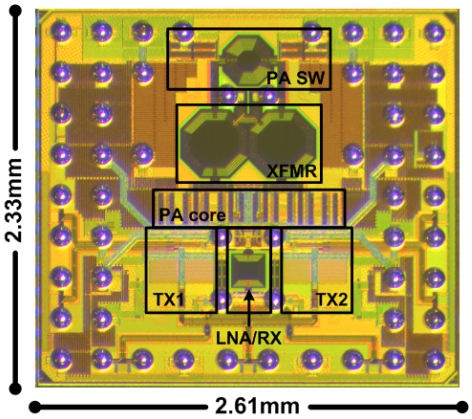


Fig. 7: Chip micrograph of implemented TDD system.

IV. Measurement Results

A system prototype was fabricated in TSMC 65nm, and a chip micrograph is shown in Fig. 7. The chip is flipped directly onto PCB with no package, and PCB traces have been de-embedded from all reported results. The chip measures 2.31mm x 2.61mm but is pad-limited. Assuming that the PA, LNA, and front-end transformer exist in comparable TDD front-ends, the area overhead used to implement T/R switching functionality reduces down to the PA supply switching structure, which has active area of 0.25mm^2 including the supply transformer. All other mode switches are negligible in area in comparison.

Fig. 8 shows measured LNA S11, S21, and NF across the frequency band of interest. Including buffer, the full RX path has peak gain of 26.8dB and -3dB bandwidth of 2.7GHz. Based on simulations, the LNA's standalone gain is about 17dB. Measured noise figure, also including RX buffer, is 5.1dB at its lowest point, and the NF +1dB bandwidth is 2GHz. The measured input P1dB is -6.7dBm. The LNA consumes 9mA from 1.5V.

Fig. 9 shows measured P_{SAT} and drain efficiency across frequency. With 1.2V supply voltage, the PA achieves 32.7% peak drain efficiency at 20dBm output power at 4.2GHz. Performance greater than 5GHz could not be measured due to limitations of the measurement setup. However, existing results indicate wideband PA frequency response similar to the LNA.

Fig. 10 and Fig. 11 show the AM-AM, AM-PM, and PM-PM characteristics of the implemented transmitter, measured with 4.2GHz carrier. The compressive AM-AM behavior and the AM-PM distortion are characteristic of digital PAs and can be linearized with pre-distortion. Fig. 10 plots a measured AM-AM response after pre-distortion. The 4-quadrant curved PM-PM response is due to I/Q phase interpolation and can similarly be linearized with predistortion as shown in Fig. 11. Fig. 12 shows a QAM16 constellation measurement at 4.2GHz and with 16.4dBm average P_{OUT} as proof-of-concept for our TDD front-end. A comparison table of T/R switching front-ends is presented in Table I. This work presents the only wideband integrated TDD front-end without frequency tuning and including full TX, while achieving comparable performance to narrowband systems.

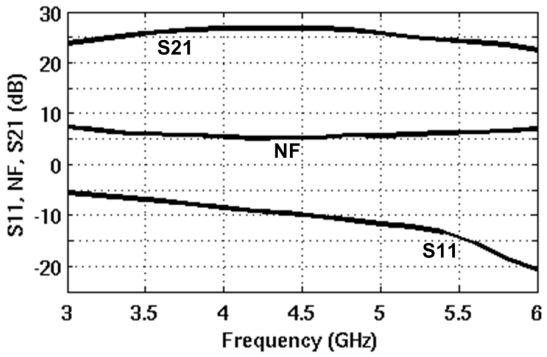


Fig. 8: Measured LNA performance across frequency.

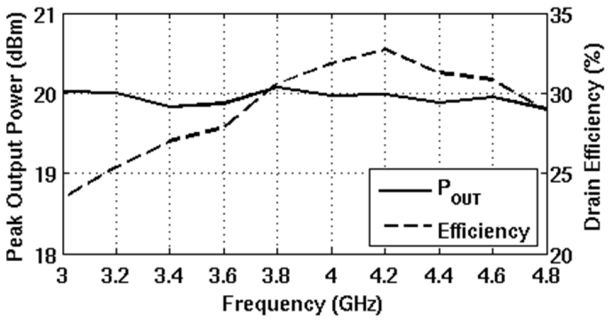


Fig. 9: Measured PA performance across frequency.

TABLE I: Comparison Table.

	[2]	[3]	[5]	[8]	This Work
Architecture	SW +LNA	SW +LNA	SW+PA +LNA	SW+PA +LNA	SW+TX +LNA
Technology	180nm	32nm	45nm SOI	90nm	65nm
Freq. (GHz)	2.5	2.5	1.4-3.4[1]	5.2	3.4-5.4
LNA NF (dB)	3.0	3.5	2.8-6.0	3.2	5.1-6.1
LNA P1dB (dBm)	-6	-5	-[2]	-13	-6.7
LNA Power (mW)	23.1	19.8	6.0	15.3	13.5
PA Psat (dBm)	-[3]	-[3]	27.6	25.9	20
PA Eff. (%)	-[3]	-[3]	30[4]	26.7[5]	32.7

[1]With frequency tuning. [2]IIP3 = -7dBm
[3]No PA in system. [4]Includes PA drivers. [5]PAE

V. Conclusion

A TDD front-end implementing a substantially different PA re-use T/R switching technique has been presented. Integrated wideband TDD co-existence at RF frequencies is achieved with no series RF switches in the signal path. Instead, only low-frequency mode control switches are used. This work contributes a key innovation towards greater front-end integration and reconfigurability for modern and future multi-band radios.

Acknowledgment

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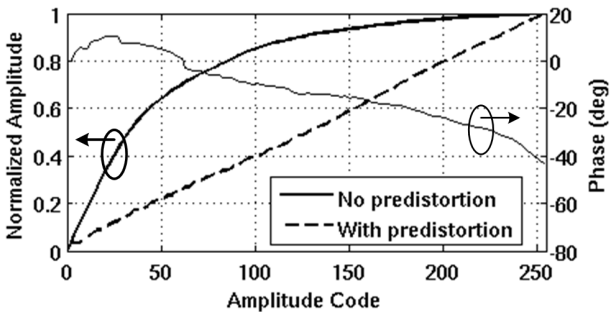

Fig. 10: Measured PA amplitude and phase vs. AM code.

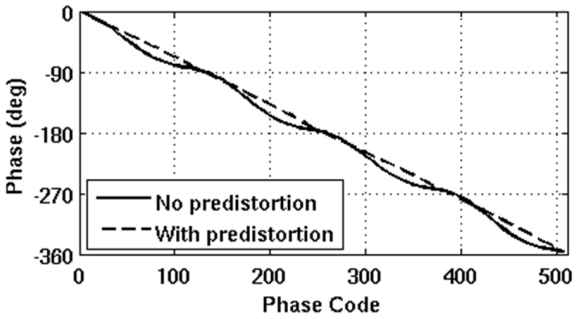

Fig. 11: Measured PA phase vs. PM code.

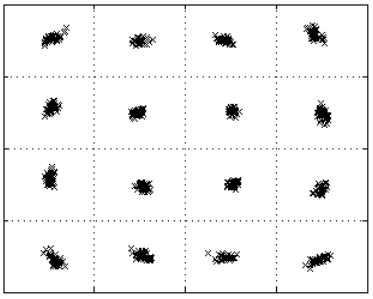

Fig. 12: Sample measured QAM16 constellation.

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