Design insights for reliable energy efficient OxRAM-based flip-flop in 28nm FD-SOI

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Abstract - This paper investigates the design architecture and the optimum resistance state values for high-endurance, high-yield energy-efficient OxRAM-based non-volatile flip-flops (NVFF) for ultra-low power applications in 28nm FD-SOI. Silicon measurements demonstrate that a low programming current improves endurance, but at the expense of a reduced memory window (R_{OFF}/R_{ON}). Statistical analyses show that the scaling limitation of the NVFF operating voltage in restore mode can be overcome with a narrow memory window by using a current-based design solution. Low variability of the FD-SOI enables to operate down-to 0.7V with more than 10^8 of endurance cycles.

I. Introduction

Integrating back-end-of-line (BEOL) non-volatile memories (NVM) in a logic process paves the way for "zero consumption" in sleep mode for ultra-low power applications, while enabling system state saving and fast wake-up transition. In this framework, several non-volatile flip-flop (NVFF) designs have been reported, connecting NVM devices to the master or slave latch with current [1] or voltage restore [2] mechanisms. Among BEOL NVM, OxRAMs appear as a key enabling technology for non-volatile circuit design due to its simple stack architecture, high scalability, fast programming time at low voltages and CMOS BEOL compatibility [3]. However, the variability of both OxRAM and CMOS devices can compromise the use of NVFF for large scale integration, especially for low-voltage applications. This paper focuses on the optimum R_{OFF}, R_{ON} state values to achieve low-voltage and reliable NVFF designs in 28nm FD-SOI.

II. ReRAM Electrical Specifications

Fig.1 demonstrates that the R_{ON} and R_{OFF} values can be adjusted by tuning the SET current compliance (I_{COMP}) and the RESET voltage (V_{RST}), respectively. The silicon data have been measured on several tens of HfO2/Ti OxRAM devices described in [4-5] through 500 SET/RESET programming cycles to capture both spatial and cycle-to-cycle variations. For a higher number of cycles, Fig.2 and 3 show that lowering I_{COMP} improves the device endurance and reduces the programming consumption, but at the expense of a higher R_{ON}. The lower memory window can be compensated with a higher V_{RST} that allows R_{OFF} to be increased. Maximizing the SET and RESET voltages also favorably lowers the programming energy (Fig.4) due to exponential dependency of switching time on the programming voltage. However V_{RST} cannot exceed 1.5V to limit the electrical stress amplitude [6]. These measurements therefore highlight that a trade-off exists between endurance, programming energy and memory window. Consequently, the NVFF performance and robustness are related to this trade-off. Especially, NVFF has to be designed in order to ensure reliable restore margin, which is sensitive to CMOS variability, within the available memory window.

III. Reliable Low-Voltage NVFF Design

Typical NVFF (Fig.5(a)) consists of a non-volatile block connected to the slave of a regular master-slave flip-flop. In store operation, the two NVM devices are programmed in accordance with the value of the internal nodes of the latch, Q/Q_b. To recover the data during restore operation, the resistance difference is sensed and amplified by the slave latch. Working with small signals, the NVFF yield then depends on the restore operation robustness. The latter is the function of the resistance values, restore mechanism, slave stage architecture and CMOS variability. Moreover, in 28nm NVM access transistors are stacked (Fig.5(b)) for protection of CMOS devices since the expected programming voltages go beyond reliable range [2], impacting the restore yield by increasing CMOS parasitic resistances.

Fig. 6 depicts the three compared design solutions: voltage-restore unbalanced latch where the NVM devices are tied to *Qb*/*Q*; voltage-restore balanced latch with symmetrical branches; and current-restore balanced latch where the NVM devices are tied to the sources of the NMOS transistors of the latch. In the following, bit error rate (BER) of the cells is estimated for various R_{ON}, R_{OFF} values by performing 10000-sample MC simulations of restore operations (both cases – restore "1" and restore "0"), including CMOS variability.

In a restore operation, *Q*/*Qb* are initially precharged then released for restoring data. Due to lower PMOS resistance, for the voltage-restore unbalanced latch charging node *Q* is faster than *Qb*, favoring 1 over 0. Fig.7 shows the 0-restoration BER versus R_{OFF}/R_{ON} ratio extracted for two R_{ON} values. Results show that for a same ratio, higher resistance values enable better yield by reducing the impact of the parasitic NVM access transistor resistance. Extracted (R_{ON}, R_{OFF}) pairs at 3σ yield (Fig.8) demonstrate that balancing the structure significantly reduces the memory window required for a same yield and that current restore outperforms the voltage-restore architecture. As described in Fig.9, restore@0.7V is successful for R_{ON} of 3-5kΩ and R_{OFF}>30kΩ, which is compatible with OxRAM programming conditions of I_{COMP}=140uA and V_{RESET}=1.5V (Fig.1), enabling 10^8 endurance cycles. Restore@0.8V and higher requires R_{ON} in 4kΩ-10kΩ range for 70uA of I_{COMP}, resulting in lower programming energy. Finally, the same NVFF is simulated in 28nm BULK CMOS (Fig.10), raising the minimum restore voltage at 1V demonstrating the benefit of FD-SOI low variability for low voltage operations.

IV. Conclusions

The current restore operating mode relying on a quasi-symmetrical latch is demonstrated as the most efficient NVFF design to face OxRAM variability. Reliable on a narrow memory window, it allows both high OxRAM endurance and low data programming consumption. 28nm FD-SOI enables the operation down to 0.7V with more than 10^8 endurance cycles which is adequate for nominally-off instantly-on systems.

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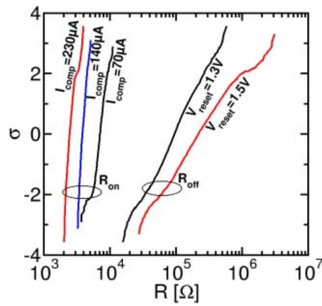

Fig 1. Experimental resistance value distribution versus programming conditions (R_{ON} vs I_{COMP}, R_{OFF} vs V_{RST}) for the HfO2/Ti OxRAM depicted in [4].

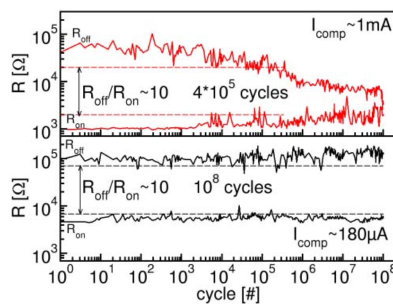

Fig 2. Experimental Pulse cycling endurance test for a SET compliance current (I_{COMP}) of 1mA (top) and 180μA (bottom). Pulse width = 10μs.

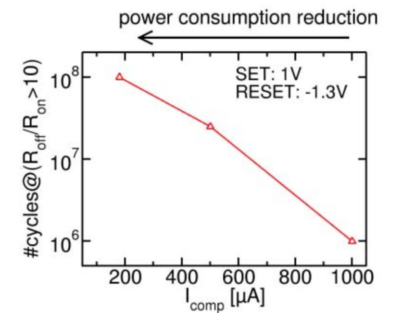

Fig 3. Endurance evolution versus the SET compliance current (I_{COMP}) values.

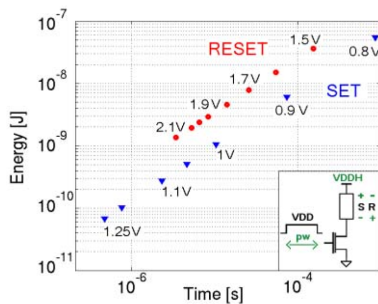

Fig 4. Simulated SET/RESET energy versus switching time for various voltage (VDDH) across the cell shown in the inset.

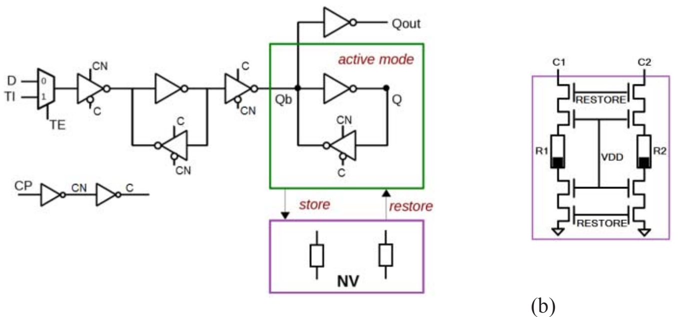

Fig 5. (a) NVFF operation principle (b) transistors of NV part are stacked for 28nm CMOS reliability as in [2]; C1/C2 nodes connect NV and slave stage

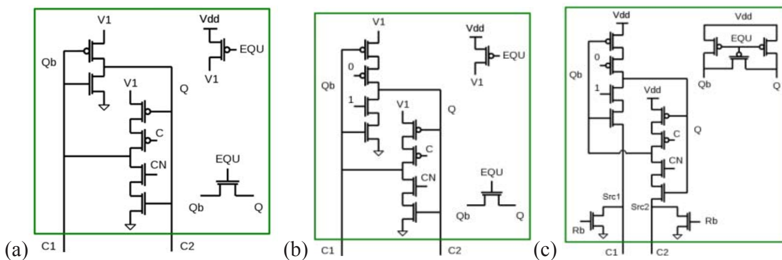

Fig 6. Schematics of: (a) voltage-restore unbalanced latch; (b) voltage-restore balanced latch; (c) current-restore balanced latch;

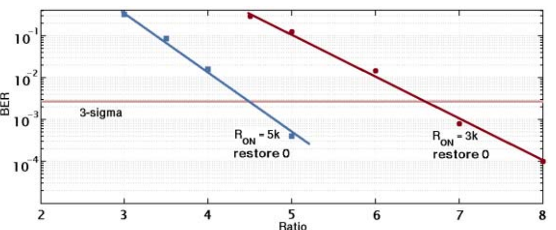

Fig 7. Restore BER versus R_{OFF}/R_{ON} ratio of the voltage-restore unbalanced latch for R_{ON} = 3kΩ and R_{ON} = 5kΩ

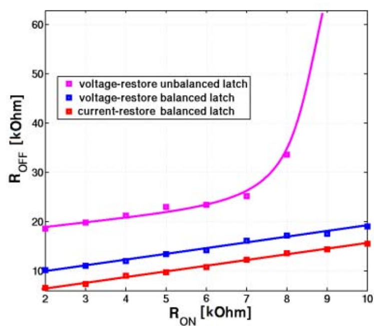

Fig 8. Restore memory window (R_{OFF}, R_{ON}) extracted at 3σ yield for the 3 latches depicted in Fig. 6.

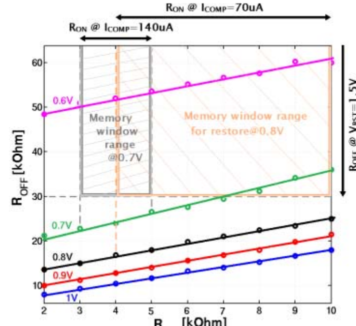

Fig 9. Restore memory window evolution versus supply voltage extracted at 3σ yield for the current-restore symmetrical NVFF.

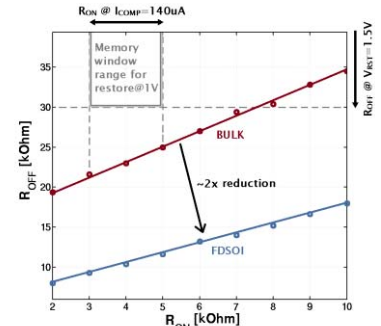

Fig 10. Comparison of bulk and FD-SOI restore memory window extracted at 1V for the current-restore symmetrical NVFF.