A 550-2260MHz Self-Adjustable Clock Generator in 28nm FDSOI

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***Abstract*—A self-adjustable clock generator that closely tracks the voltage dependence of the critical path delay in a microprocessor is presented. Real-time frequency modulation performed by a tunable replica circuit (TRC) reduces the response time to a single cycle, by picking the appropriate phases of the delay-locked loop (DLL). The generator has wide tuning range of 550 – 2260 MHz at 1V supply voltage, works down to 35 MHz at 0.4V supply, and can continuously synthesize the clock signal for arbitrary voltage waveforms between 0.4V and 1V. The proposed design was implemented in a 28nm FDSOI, and occupies an area of 1120μm^2 with 2.7mW of power consumption.**

Keywords—Adaptive Clocking, Dynamic Frequency Scaling, Delay Locked Loop (DLL)

I. Introduction

Dynamic-voltage-frequency-scaling (DVFS) relies on accurate tracking of the critical path in a digital system to maximize the operating frequency at each supply voltage. Real-time frequency adaptation in microprocessors also reduces supply noise voltage margins [1]. Per-core setting of supplies and frequencies is particularly important for the efficiency of multi-core systems by adjusting the timing margin, and thus reducing the energy consumption of each core separately. For maximum energy efficiency, in addition to accurately tracking the critical path of a system, it is necessary to design the clock generator to adapt to the supply changes in the shortest time.

Current approaches for clock generation include the use of integer dividers, per-core analog or digital PLLs, prescalers with DPLLs or a main PLL with per-core DLLs [2-5]. These adaptive techniques detect the supply droop using the analog droop sensor, determine the operating condition, and adjust the clock frequency accordingly. The entire response time can be up to several clock cycles because the digital controller needs time to calculate the new target frequency. To reduce the response time, additional resources (e.g., multiple PLLs) may be applied, but this increases area and power consumption.

Another adaptive clocking technique [6] reduces the adjustment time through direct modulation of the PLL's clock frequency by using the supply voltage change. This approach requires simpler logic and shortens the response. However, it has a local PLL for tracking the voltage droop which requires additional locking time whenever the voltage droop happens, and extra area.

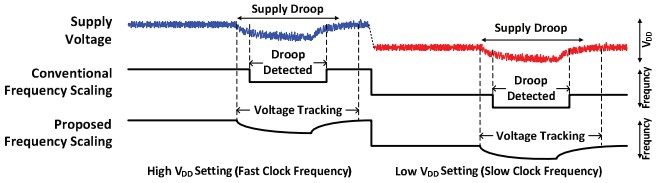

Fig. 1. Conventional frequency scaling vs. proposed frequency scaling

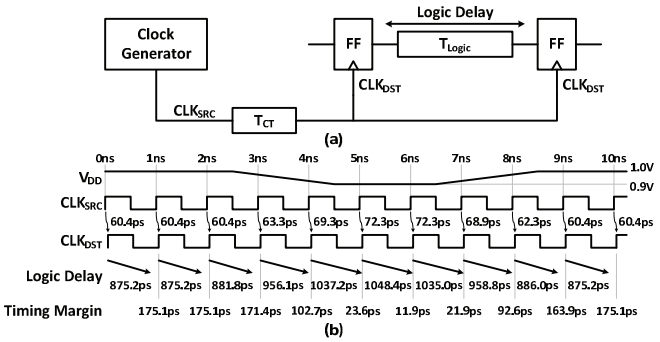

Fig. 2. (a) Conventional clock tree and the logics, and (b) its timing diagram with the delay annotated.

This paper presents an self-adjustable and low-area clock generator with a very fast response time. The proposed clock generator adapts to the rapidly varying supply voltage, while the conventional generators target the constant supply voltage, and detect the unwanted voltage droop. By removing droop detection and tracking the droop, per-cycle frequency adjustment can be achieved with small area.

II. Principle of Operation

The clock frequency in a DVFS system not only needs to respond to the externally set frequency targets, but also needs to track the supply voltage droops caused by load variations. The conventional frequency adjustment schemes do not track the continuous droop, and rather apply a discrete frequency step, as shown in Figure 1. The proposed clock generator adapts to the continuously varying target voltage, and changes the frequency by directly applying the varying supply to the replica circuit that generates the clock period.

Real-time frequency adjustment is essential for the energy efficiency of the processor. If the clock source generates a fixed frequency, the timing margin (data-to-clock delay, T_{DC}) under nominal conditions has to be large to guarantee adequate cycle time for worst case supply noise. A simulation model shows the timing margin at each clock rising edge (Figure 2).

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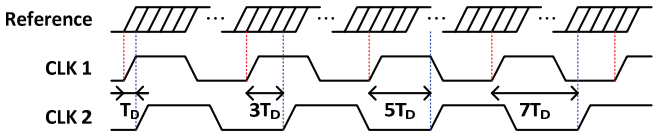

Fig. 3.The clock skew between two clock signals which are generated from the same reference (T_D is the resolution of the reference.)

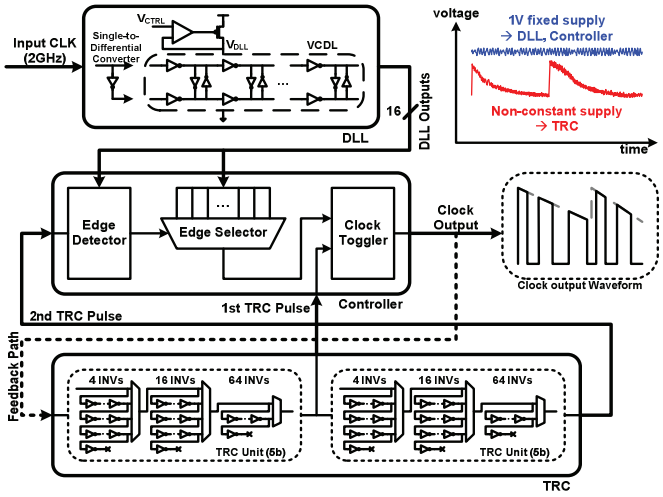

Fig. 4. Block diagram of the proposed clock generator

The clock frequency is set to 1GHz, and the logic path is adjusted to have 1.2% of timing margin at 0.9V. At nominal operating conditions of 1V, design margins account for 17% of the clock period.

If per-core DVFS is applied to a multicore processor, the synchronization latency between two clock domains can degrade the performance. The conventional approach to synchronization requires 2-3 stages of flip-flops in series, regardless the of clock skew. By quantizing the skew between two clocks, the synchronization latency can be reduced to 1-2 cycles. In the Figure 3, the skew between CLK1 and CLK2 is varying but deterministic, and the latency can be adjusted based on the skew.

III. Clock Generator Architecture

A block diagram of the proposed clock generator is shown in Figure 4. The clock generator has a DLL, a tunable replica circuit (TRC), and a controller. Using the reference signals from the DLL and the estimated clock delay from TRC, the control logic generates the clock output signal by selecting one of the DLL outputs. To place and route the clock generator directly in the processor core the standard cells are used for most blocks, and the custom cells conform to the standard cell design rules.

A. Delay Locked Loop(DLL)

The schematic of the DLL is shown in Figure 5(a). The main blocks are the voltage-controlled delay line (VCDL), the phase detector (PD), and the charge pump (CP) with the loop filter (LF). The DLL uses a constant 1V supply to isolate itself from the main system's varying supply.

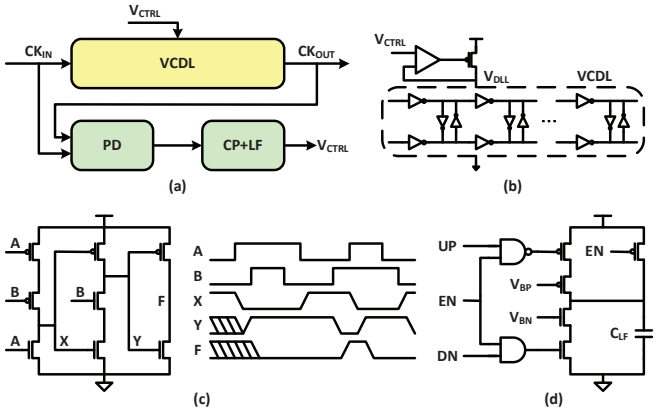

Fig. 5. (a) Block diagram of the DLL, (b) the voltage-controlled delay line, (c) the phase detector, and (d) the charge pump with the loop filter

The VCDL converts a single-ended 2GHz clock signal into 8 differential signals of the same frequency. All 16 reference signals have the same interval of 31.25ps (= 500ps/16), and they are controlled by a low-dropout (LDO) regulator. The VCDL generates 16 phase references, where the 16th phase matches the input phase of the clock. To minimize the phase mismatch of the input pair of the VCDL, a single-ended to differential converter is composed of an inverter followed by two differential pairs. Since the output voltage level of the VCDL, which is controlled by the local LDO, is usually lower than a nominal voltage (1V), a level shifter is added to each output signal. The level shifter is followed by a large buffer to minimize interval mismatch between adjacent outputs of the VCDL due to the load mismatches. Decoupling capacitors reduce the voltage ripple at the VCDL.

The phase detector compares the phases of the reference clock and the output. The output F is set to '1' only when the input B rises faster than the input A, and stays high until the input A is on. The pulse width of the output F is a function of the time difference between the two rising edges. In the DLL, the 16th reference is connected to the input B, while the 0th reference is to the input A. The charge pump determines the reference voltage level of the LDO. The 10fF of capacitance is placed at the output of the CP as a loop filter. This charge pump also has a reset signal (EN), so the output goes up to 1V if the signal is asserted.

B. Tunable Replica Circuits (TRC)

The tunable replica circuit shown in Figure 6 is designed as a configurable inverter chain, and has two units that are independently controlled to set the duty cycle of the output clock. Each unit consists of 124 inverter cells of same size with 5 bits control signals, and the configuration resolution is 4FO1 delays, where FO1 is the fanout-of-one inverter delay. The first unit is for the high phase of the clock, which starts at the rising edge and generates the falling edge, while the second unit is for the low phase, vice versa. With this feature, the period and the duty cycle can be independently adjusted. Two TRC units of 5-bit control each are equivalent of 6-bit control delay chains, resulting in a very wide tuning range of 0 to 248 FO1 inverter

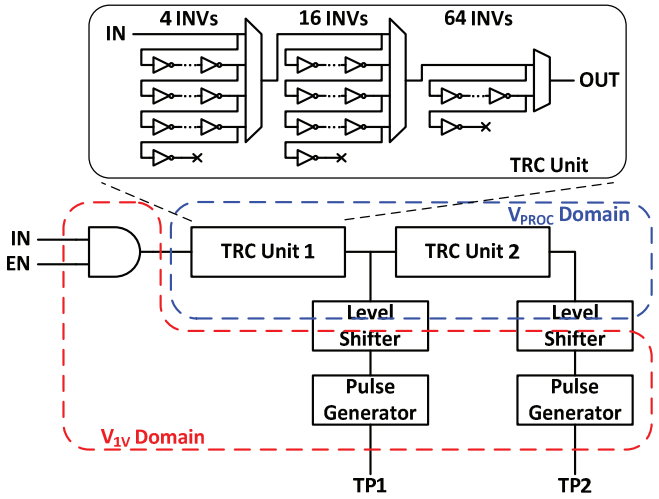

Fig. 6. Block diagram of the tunable replica circuits (TRC)

delays. The TRC inverters are connected to the processor supply (V_{PROC}) in order to track the critical path under voltage noise, while other logic remains in an isolated 1V domain (V_{1V}). Therefore, 4FO1 resolution is guaranteed at any supply voltage level, while the total delay is self-adjusted as a function of the supply. We chose the variable resolution along the supply rather than a constant resolution because the number of FO1 (as well as FO4) is used to measure the performance of the microprocessor regardless the voltage level.

At the top level, the output clock signal is connected to the TRC input, which is sent to the microprocessor as well. Two TRC units delay the rising edge of the input successively by the estimated critical path of the processor through appropriate digital calibration of the number of delay stages, and convert the delayed edges to short period of pulses using the pulse generators (PG) for the controller. The level shifters are located between the TRC and the PG, because the TRC units use the microprocessor's voltage domain while the PG and the controller operate at 1V. The TRC goes into sleep mode to reduce the energy consumption when not in use by de-asserting the enable signal (EN). Since the TRC delay directly determines the next clock period without any additional logic that takes extra clock cycles, a single clock cycle of response time is achieved.

C. Controller

The controller is composed of an edge detector, an edge selector, and a clock flip-flop as shown in Figure 7. The DLL references and the TRC pulses are used in this block. The clock output signal is generated from the flip-flop followed by a large clock buffer. The flip-flop has a data input connected to V_{DD}, an asynchronous reset input connected to the first TRC output pulse, and a clock input from the edge selector. The first TRC output pulse asynchronously reset the flip-flop to generate the falling edge of the clock output. The second TRC output pulse, however, is not directly used to generate the rising edge because the rising edge should be synchronized to the DLL references. In the edge detector, the second TRC output pulse samples the DLL references to detect a reference

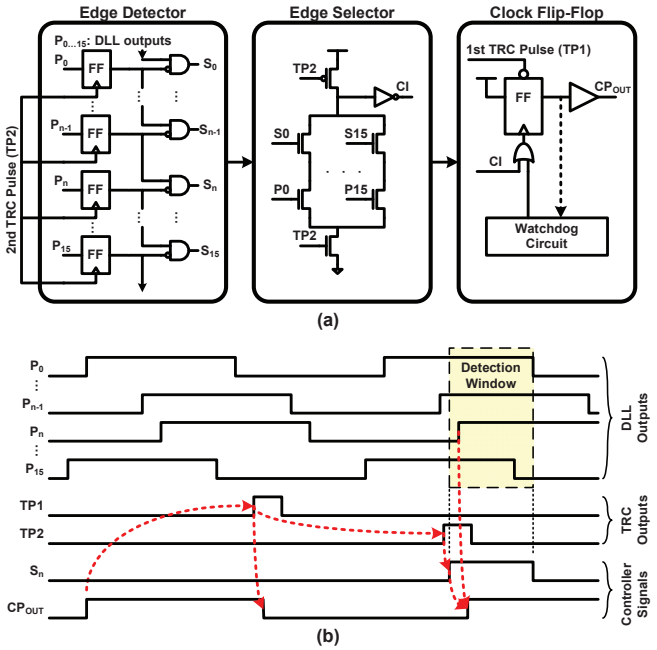

Fig. 7. (a) Controller architecture, and (b) clock output generation

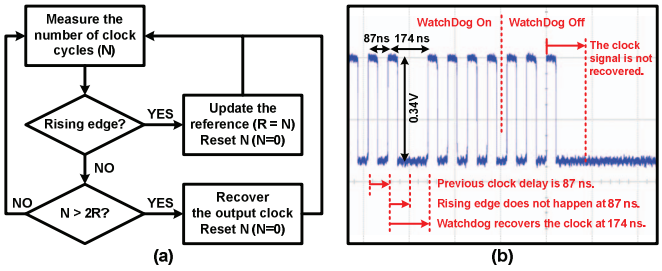

Fig. 8. (a) Watchdog flowchart, and (b) its measurement result

phase that is about to rise. Since the reference signals have equivalent intervals, the sampled values are eight continuing 0's and eight continuing 1's circularly, and the first 0 after the sequence of 1's corresponds to the phase of upcoming rising if no meta-stability happens. The edge selector picks the correct reference phase by using the result from the previous stage. The dynamic MUX gate is used to improve the operation speed. The gate is in the evaluation phase only when the second TRC output pulse is high, and goes into the precharge phase when the pulse from TRC is off. The MUX output, which is a pulse, triggers the flip-flop as a clock signal.

Since the DLL references and the TRC output pulse are fully asynchronous, the flip-flops in the edge detector may occasionally fail to sample the inputs, resulting in metastability. In most cases, the metastable outputs are resolved to '0' or '1' in a short time, so the entire operation remains correct. However, the control logic can malfunction if outputs are metastable during the period, and the clock output signal is eventually set to zero. To avoid this, a watchdog block is implemented. This logic continuously monitors the status of the clock output signal, and generates an extra pulse for the clock flip-flop input when the clock output signal remains zero for longer than two clock delays of the previous period as shown in Figure 8.

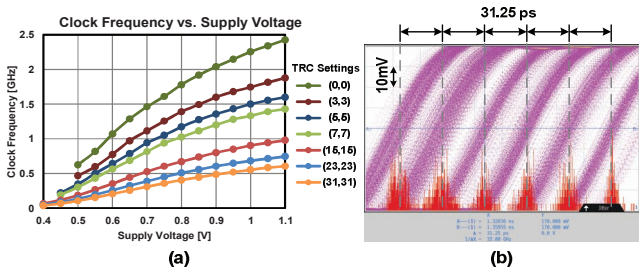

Fig. 9. (a) Clock frequency vs. voltage level, and (b) distribution of the rising edge of the output clock

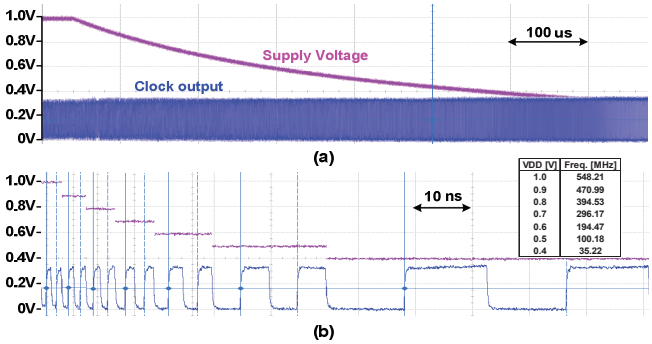

Fig. 10. Clock frequency vs. supply voltage droop: (a) entire waveform, and (b) zoomed waveform of selective points

IV. Experimental Results

The clock generator has been fabricated in a test chip shown in Figure 11 implemented in 28nm ultra-thin body and BOX fully-depleted silicon-on-insulator (UTTB FDSOI) technology [8]. The clock generator macro is implemented with custom-placed standard cells for seamless embedding into designs. It occupies an area of 1,120µm^2, and consumes 2.7mW from 1V supply.

Figure 9(a) shows the tuning range of the generator. At 1V, the frequency range of 550–2260MHz can be achieved depending on the TRC configuration. The TRC delay, which determines the clock frequency, is longer at lower supply voltages, and thus the frequency range scales down to 103–625MHz at 0.5V. Since the clock output is generated from the DLL outputs, the rising edge of the clock has a discrete distribution same with the DLL outputs distribution of 31.25ps interval, verified by the plot in Figure 9(b).

Figure 10 shows the frequency change when the supply decreases from 1V down to 0.4V. Selected points (0.4V to 1.0V, 0.1V step) illustrate the clock frequency changes, and the frequency of each selected point follows the trajectory in Figure 10(a). The clock generator has been verified to operate down to 0.35V. If the supply is below 0.35V, the clock generator fails to generate the stable signal, and the watchdog logic resurrects the clock output. Figure 8 shows the clock signal at 0.34V is revived when the watchdog is activated, but remains zero when deactivated.

This clock generator has been embedded in a dynamic voltage scaled processor as well, where it has been demonstrated to track the supply droops that exceed 100mV, and improve the overall energy efficiency by more than 10% [7].

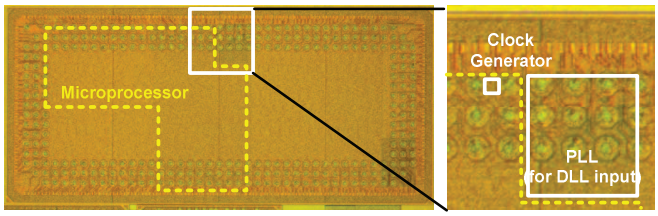

Fig. 11. Chip micrograph

Table 1. Design summary and comparison with previous works

Parameter	This Work	[2]	[3]	[4]	[5]
Technology	28nm FDSOI	28nm FDSOI	28nm Bulk	45nm PDSOI	90nm CMOS
Size [mm^2]	0.000112	0.098	N/A	0.07	0.75
Minimum Frequency	35MHz at 0.4V	1MHz at 0.33V†	2.0GHz at 0.86V	1.8GHz at V_{NOM}	2.2GHz at 1.0V
Maximum Frequency	2.26GHz at 1.0V	443MHz at 0.9V	4.0GHz at 1.45V	4.0GHz at V_{NOM}	3.4GHz at 1.4V
Power	2.7mW at 1V	5mW at 0.45V	N/A	N/A	N/A

† 0.8V FBB (Forward body biasing) is applied.

V. Conclusion

The rapidly-adjustable clock generator in this paper has wide voltage range of 0.4 - 1V, and synthesizes the clock signal of 35-2260MHz. The design, including DLL, TRC, and controller, was implemented in a 28nm FDSOI process, and has small size of 1,120µm^2. The clock generator can be used to reduce margins against voltage noise in a wide variety of applications.

Acknowledgment

The author acknowledge BWRC, ASPIRE, Brian Richards, Brian Zimmer, and Yunsup Lee. This work was funded in part by DARPA PERFECT Award Number HR0011-12-2-0016, SRC/TxACE 1836.136, Intel, KFAS Fellowship, and fabrication donation by STMicroelectronics.

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