A Dual-Mode, Correlation-Based Spectrum Sensing Receiver for TV White Space Applications Achieving -104dBm Sensitivity

Xiao Xiao, Borivoje Nikolic

University of California, Berkeley, CA, 94720

***Abstract* — A spectrum-sensing receiver targeted at the UHF TV band is implemented in 65nm CMOS. Using known characteristics of the target signal, an efficient architecture employing subsampling downconversion and digital-analog hybrid correlation is implemented to achieve high sensitivity with low power. Fine and coarse detection modes enable both rapid sensing and the detection of very weak signals. For a 6MHz TV band channel, the system achieves -91dBm sensitivity with rapid energy detection, -104dBm sensitivity with correlation, and 84dB of full-scale dynamic range. The chip consumes only 28mW of power.**

***Index Terms* — Cognitive radio, correlation, energy detection, spectrum sensing, sensitivity, TV white space.**

I. Introduction

As mobile data usage is expected to increase exponentially in the coming years, cognitive radios have been proposed as a possible solution to the resulting problem of spectrum scarcity. The cognitive radio allows unlicensed users to use licensed bands on a secondary basis, but in order to guarantee non-interference, this requires robust sensing of the spectrum to accurately determine the presence, or lack thereof, of a primary user. The difficulty of spectrum sensing arises from the high sensitivity requirement which is more stringent than that of a standard receiver, as well as a high dynamic range in order to sense high-powered signals and tolerate blockers.

In previous works which implement spectrum sensing functionality in mobile receivers, many had limited sensitivity comparable to or worse than that of a conventional mobile TV tuner [1][2], making them suitable only for coarse scanning through the band. Other solutions were not fully integrated; for example, only the RF front end was implemented on-chip in [3]. Realizing both high sensitivity and high dynamic range in an integrated, low-power form factor has not been demonstrated in state-of-the-art.

We present a spectrum-sensing receiver that uses coarse and fine detection methods to trade off sensitivity and scanning time. Energy-based sensing is used in the coarse mode, while subsampling downconversion and digital-analog hybrid correlation are used to achieve a maximum sensitivity of -104 dBm and a dynamic range of 84 dB in the fine mode. This work is targeted at spectrum sensing in the 400MHz to 700 MHz UHF TV band, which in the U.S.A. has been approved for cognitive radio operations.

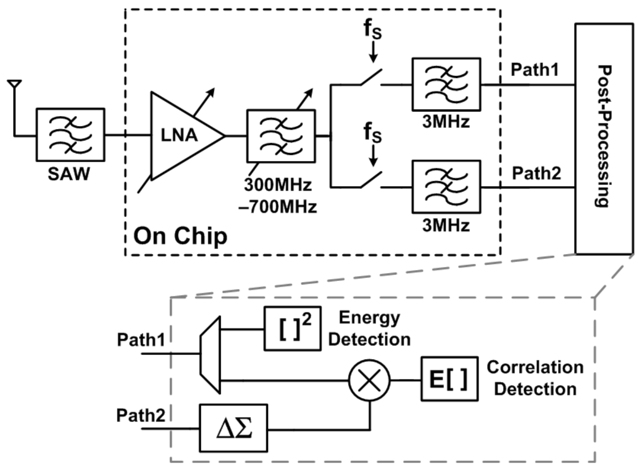

Fig.1. Block diagram of spectrum sensing system.

II. Proposed System

A block diagram of the target system is shown in Fig. 1. Strong blockers from the neighboring GSM bands are removed with an off-chip SAW filter. A single RF front-end provides amplification and band filtering before the signal splits into two identical paths. In each path, a sampler is used to directly downconvert the signal to baseband. Blockers at the 2nd and higher clock harmonics fall out of band and are removed with the front-end SAW filter. The sampling clocks are ideal and routed from off-chip. Following downconversion, baseband filters provide channel selection, and the filtered baseband outputs are then processed off-chip.

A. Dual-Mode Detection

Coarse and fine detection modes, implemented respectively as energy detection and correlation, allow efficient sensing of a wide dynamic range of input signals. Energy detection simply measures the received power. This mode in practice would be used for a fast, coarse scan of all channels to eliminate ones with strong signals. Correlation, being more time consuming, would then be used on a few likely-vacant channels where the signal, if present, is too weak to be sensed with energy detection.

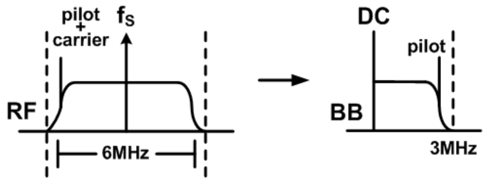

Fig.2. A 6MHz ATSC signal is converted to 3MHz at baseband.

In correlation mode, the signal from the two baseband paths are multiplied and then averaged. This causes uncorrelated sampling and baseband noise to be eliminated, drastically reducing the effective noise contribution of the system. A single shared RF front-end path was chosen for power efficiency and for ease of input impedance matching.

B. Subsampling Downconversion

The UHF TV band in the U.S. consists of 6 MHz channels with vestigial sideband modulation. A sinusoidal pilot tone is placed 310kHz above the lower channel edge, which is also the frequency of the buried carrier. To perform downconversion, the proposed system uses a low subsampling ratio of 1 to minimize noise folding, and a sampling frequency equal to the center, not carrier, frequency of the desired channel, as shown in Fig. 2. This approach has several advantages.

First, it enables direct conversion of the channel and eliminates any need for image rejection. Second, the pilot tone falls to the low-IF frequency of 2.69MHz and can be detected within its narrow bandwidth as an alternate detection mode. Third, the channel at baseband folds onto itself and becomes only 3MHz wide. Due to this folding, the channel data becomes corrupted and undecodable, but this is acceptable for our application as we only wish to sense the presence of the signal in the channel.

C. Hybrid Correlation

The high-resolution, high-linearity multiplication operations required for correlation are complex and power-intensive in both analog and digital implementations. This complexity can be significantly reduced if signals were instead converted to sigma-delta bitstreams prior to correlation. However, two bitstreams have correlated out-of-band quantization noise that will mix to DC and severely degrade in-band SNR. Instead, the analog-digital hybrid correlation scheme from [4] is employed. In this method, only one signal path is turned into an oversampled bitstream with a sigma-delta modulator, as shown in Fig. 1. When correlated with an analog signal, the quantization noise is uncorrelated and removed, while the SNR fidelity of the correlation is preserved as comparable to ideal analog correlation.

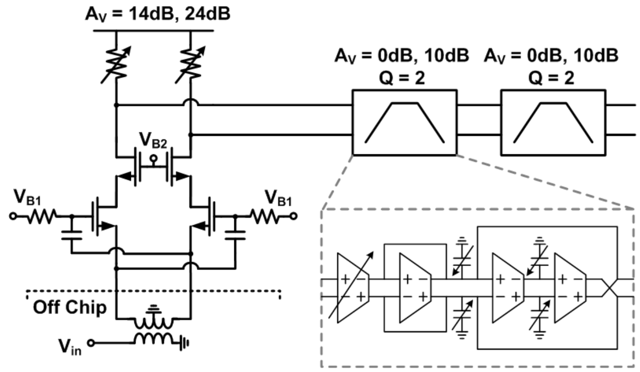

Fig.3. Schematic of RF front end.

III. Circuit Implementation

A. RF Front End

The RF front end, shown in Fig. 3, needs to have high gain and low noise figure to meet the high sensitivity requirement, but it must also have adequate linearity and tunable gain for good dynamic range. The LNA uses a capacitively cross-coupled common gate architecture to present a wideband impedance match to a 50Ω antenna. This topology also provides an optimal trade-off between gain, linearity, and noise figure. The LNA has one bit of tuning in its resistive load to enable high and low gain.

The RF filter is a 4^{th} order bandpass filter implemented with a cascade of two Gm-C biquads. The filter has tunable center frequency from 300MHz to 700MHz, as well as tunable gain. The total RF front end gain is programmable from 14dB to 44dB. The RF front end noise figure in its highest gain setting is 3.5dB. The LNA consumes 7mW while the RF filter consumes 12.3mW.

B. Sampler and Baseband Filter

Fig. 4 and Fig. 5 illustrate the sampler and the baseband filters. The sampler used to enable downconversion consists of two sample-and-hold stages clocked on the opposite phase, with gate bootstrapping on the sampling switches to maximize linearity [5]. The sampler is followed by a 4th order lowpass Chebyshev baseband filter to provide channel selection at 3MHz. The baseband filter is implemented as a cascade of two Tow-Thomas biquads with a DC servo loop to attenuate flicker noise. The samplers consume 2.5mW at 500MHz sampling frequency, and the baseband filters consume 5.2mW.

The baseband filter is able to reject 37dB at the adjacent channel, 60dB at the N+2 channel, and greater than 70dB for N+3 and beyond. Given the blocker profile of the TV band, strong in-band blockers are sufficiently attenuated to prevent desensitization of the desired channel.

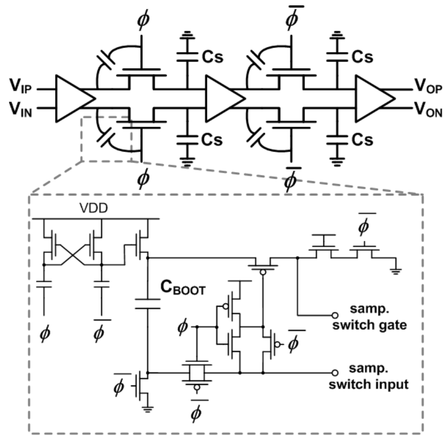

Fig.4. Schematic of sampler.

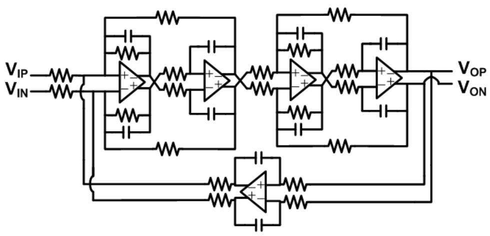

Fig.5. Schematic of baseband filter.

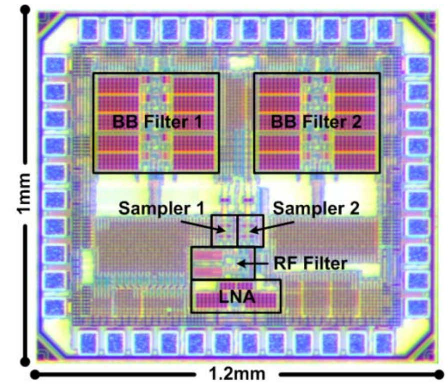

Fig.6. Chip micrograph of spectrum sensing system.

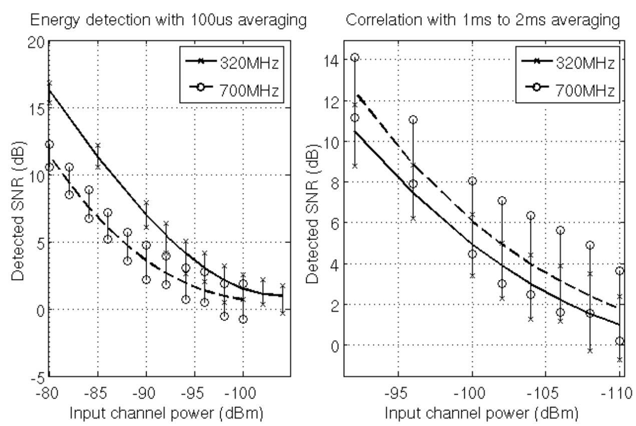

Fig.7. Measured detected SNR for energy and correlation detection modes. Error bars correspond to the maximum and minimum detected SNR over four signal and four noise samples.

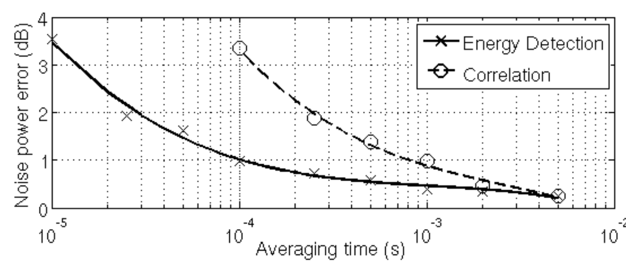

Fig.8. Convergence of noise power with averaging time.

IV. Measurement Results

A chip prototype of the system, shown in Fig. 6, was fabricated in 65nm CMOS process with a 1.2V supply. All post-processing was performed in software. At the highest gain mode, the measured input-referred noise power within the 3MHz baseband channel is -96dBm to -91dBm across the 300MHz - 700MHz RF band at room temperature. When referred to the original 6MHz RF channel bandwidth, this corresponds to a sensitivity of -164dBm/Hz to -159dBm/Hz.

In order to compare different detection modes, the detected SNR is defined as the ratio of detected channel power when a signal is present to detected channel power when no signal is present. The sensitivity is defined as the input signal power at which detected SNR reaches 3dB, where signal power equals noise power. Robust sensing, however, is possible at lower detected SNR thresholds with accurate noise estimation algorithms.

Fig. 7 shows detected SNR as a function of input power in the highest gain mode. For energy detection, the 3dB detected SNR point occurs at input powers of -96dBm to -91dBm, which, as expected, matches the channel noise power. With correlation, a sensitivity of -104dBm to -106dBm was achieved at room temperature. All measurements were performed with a single tone at the pilot frequency, and include the insertion loss of the off-chip balun and SAW filter.

Detection speed is determined primarily by the amount of time necessary to average enough noise samples for a robust estimation of noise power. Fig. 8 shows the convergence of noise power over time for energy and correlation detection. The total noise power is determined by averaging a 20ms sample, and noise error is defined as the maximum deviation from that value for each shortened averaging time. As expected, energy detection converges much faster, reaching an error of 1dB with an averaging time of about 100µs. Correlation, on the other hand, needs more than 1ms to reach a similar level of noise error.

In the lowest gain mode, the prototype achieves a P_{1dB} of -14dBm to -20dBm across the RF band, giving a dynamic

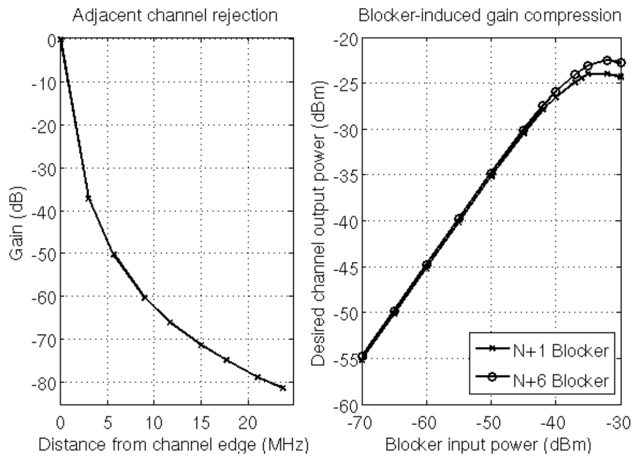

Fig.9. In-band blocker tolerance and desensitization.

range of 84dB across the full scale of gain settings. The in-band IIP3 in the lowest gain mode, measured with two tones at the N+1 and N+2 channels, is -12dBm. The out-of-band IIP3, measured with two tones at 760MHz and 860MHz, is +7dBm.

Linearity at the highest gain mode is also important as it defines when the desired channel becomes desensitized by blockers, causing the sensitivity measurement to be no longer valid. Fig. 9 shows these desensitization measurements. Due to high adjacent channel rejection from the baseband filter, blocker-induced gain compression is limited by the linearity of the RF chain. The 1dB compression point in the desired channel occurs at -42dBm blocker power for an N+1 blocker, and stays relatively constant at -40dBm for an N+6 blocker.

However, strong adjacent channel blockers also raise the noise floor of the desired channel, and this effect dominates for close blockers below N+4. Thus, desensitization due to the N+1 blocker, defined as when the desired channel noise power rises by 3dB, occurs at -58dBm blocker power. The desensitization blocker power rises to -45dBm for the N+2 blocker. Since the highest sensitivity mode is only used to detect very weak signals, and since adjacent channel power is limited to being a maximum of 27dB greater [6], this desensitization result satisfies the intended application and does not degrade the robustness of detection.

Table 1 presents a comparison to current state-of-the-art in spectrum sensing. In contrast to previous works, the presented system targets the sensing of a specific standard and takes advantage of the known characteristics of the signals in the band. By doing so, it is able to achieve the highest sensitivity for the targeted application with the lowest power of 28mW. This is achieved at expense of linearity; however, the achieved linearity is sufficient for robust spectrum sensing in the UHF TV band.

TABLE I. COMPARISON TO STATE-OF-THE-ART

	[3]		[2]	[1]	This Work
	Hi-Z	**Std.**			
Tech.	65nm		90nm	0.18 um	65nm
Freq. (GHz)	0.3-1		0.03-2.4	0.4-0.9	0.3-0.7
Detection BW (MHz)	1		0.2-30	0.025-0.8	6
Sensitivity (dBm)	-112 (1MHz)	-109 (1MHz)	-83 (150kHz)	-74 (100kHz)	-104 (6MHz)
Sensitivity (dBm/Hz)	-172	-169	-135	-124	-172
DR (dB)	– [a]	– [a]	101	32	84
IIP3 (dBm)	5	25	1.7	-17	-12
Power (mW)	36-61	41-66	30-44	119[b]	28

(a) SFDR = 89dB(Std.), 78dB(Hi-Z)
(b) Excluding VCO and PLL power

V. CONCLUSION

A spectrum sensing receiver for TV white space is presented. The receiver uses energy detection and correlation to provide both rapid and robust sensing, and is resilient against desensitization from nearby blockers. This work demonstrates the feasibility of low-power, high-sensitivity spectrum sensing for mobile receivers.

ACKNOWLEDGEMENT

This work is supported by C2S2 and NSF GRFP. The authors thank Christopher Hull for valuable advice.

REFERENCES

[1] J. Park, et al., "A Fully Integrated UHF-Band CMOS Receiver With Multi-Resolution Spectrum Sensing (MRSS) Functionality for IEEE 802.22 Cognitive Radio Applications," *IEEE J. Solid-State Circuits*, Jan. 2009.

[2] M. Kitsunezuka, et al., "A 30-MHz–2.4-GHz CMOS Receiver With Integrated RF Filter and Dynamic-Range-Scalable Energy Detector for Cognitive Radio Systems," *IEEE J. Solid-State Circuits*, May 2012.

[3] M.S. Oude Alink, et al., "Using Crosscorrelation to Mitigate Analog/RF Impairments for Integrated Spectrum Analyzers," *IEEE Trans. Microwave Theory and Techniques*, March 2013.

[4] P.H. Dietz and L.R. Carley, "Analog/Digital Hybrid VLSI Signal Processing Using Single Bit Modulators," *IEEE Workshop on Applications of Signal Processing to Audio and Acoustics*, 1993.

[5] A.M. Abo and P.R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter," *IEEE J. Solid-State Circuits*, May 1999.

[6] ATSC, " ATSC Digital Television Standard, Part 2 - RF/Transmission System Characteristics (A/53, Part 2:2007)," 2007.