A Frequency-Reconfigurable Multi-Standard 65nm CMOS Digital Transmitter with LTCC Interposers

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***Abstract*—This paper demonstrates a CMOS digital polar transmitter with flip-chip interconnection to low-temperature co-fired ceramic (LTCC) interposers. The LTCC interposers contain the PA output balun targeting different operating frequency bands, and the reconfiguration in the carrier frequency is achieved by selecting an appropriate LTCC interposer. The same CMOS core transmitter is reused for different frequency bands. In this design, an output power higher than 22 dBm from 0.6 to 2.4 GHz is demonstrated, with peak power of 27.1 dBm and peak efficiency of 52%. The polar transmitter includes 9-bit phase interpolation and 8-bit amplitude modulation, suitable and verified as a multi-standard universal digital modulator.**

***Keywords*—digital polar modulation; digital transmitter; LTCC; CMOS; power amplifier**

I. Introduction

Digital RF transmitters have been studied intensively in recent year since they can be reconfigured to cover different modulation schemes and hence provide great flexibility [1]-[4]. Due to the widely scattered frequency bands allocated for modern wireless standards, a transmitter capable of multi-standard and multi-band operation can result in significant area and component count reduction; however, currently reported digital transmitter designs are optimized for a relatively narrow frequency band.

Digital transmitters often consist of nonlinear power amplifier (PA), and the back-off operation requires the envelope elimination and restoration (EER) and the digital pre-distortion. Among the reported solutions, polar EER architecture is more popular due to a simple pre-distortion scheme and low loss in the phase synthesis, compared to the I/Q combination in the Cartesian transmitters. However, the phase modulator in the polar structures complicates the design and the signal in the phase path suffers from bandwidth expansion, which can be an issue for application targeting higher data rate and bandwidth in the future applications.

The peak power of the digital transmitter can be improved by using a higher supply voltage together with thick-oxide devices [3]-[4]. In addition, system in package (SIP) solutions [5]-[7] have also been used. Antennas, interconnections, and microwave matching networks have been fabricated on LTCC interposers to take advantage of the thicker metals and lower substrate loss. Such packages have been demonstrated up to millimeter-wave applications [7]. Also, SIP solutions are relatively low cost and have a fast fabrication turnaround.

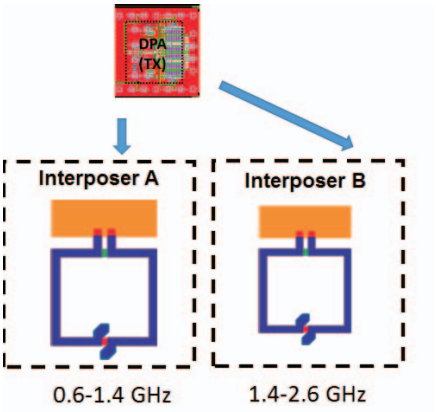


Fig. 1. Illustration of frequency reconfiguration of digital transmitter employing SIP technique.

In this work, a polar digital transmitter in 65nm CMOS is introduced with an 8-bit amplitude modulator and a 9-bit phase modulator. Frequency reconfiguration covering two frequency bands (0.6 to 1.4 and 1.4 to 2.6 GHz) is demonstrated by flip-chip packaging of the same IC onto two LTCC interposers. The two interposers differ in the output balun design to cover the frequency range of interest. The wideband phase synthesis is achieved by a Gilbert-cell-based phase interpolator (PI) [1] with built-in slew-rate-control integrators. With a 2.5 V supply, the low-band solution achieves a maximum output power of 27.1 dBm with 52% drain efficiency at 1.2 GHz, and the high-band solution outputs 24.7 dBm at 2.2 GHz with 40% drain efficiency. The digital polar modulation meets the EVM/ACLR requirements with digitally-modulated signals in multiple standards, including 802.11.ac (OFDM) and LTE UL FDD (SC-FDMA).

II. Circuit And Package Design

A. Digital Transmitter

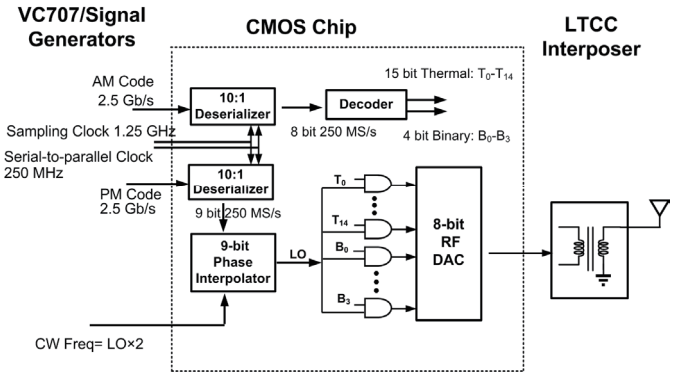


Fig. 2. Block diagram of the designed digital transmitter.

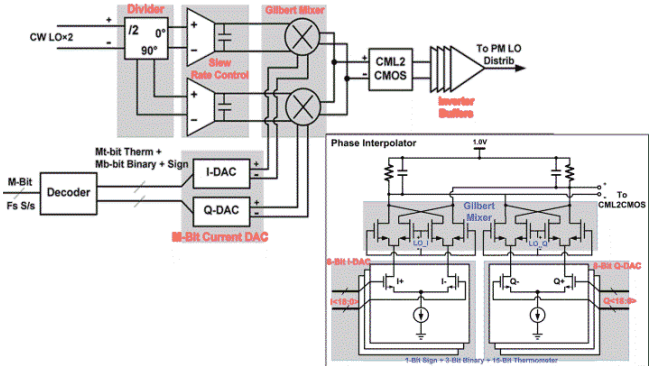
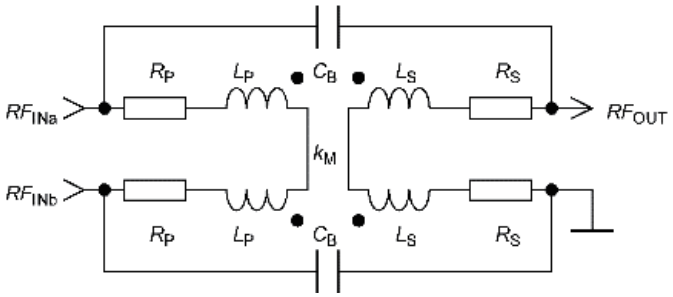


Fig. 3. Block diagram of the Gilbert-cell-based phase interpolator. (M=9, $M_{thermal}$=4, M_{binary}=5, Fs=250MS/s)

The digital transmitter is designed using the TSMC general-purpose 65nm CMOS process. The architecture, as shown in Fig. 2, incorporates an 8-bit amplitude modulator and a 9-bit on-chip phase modulator. The block diagram of the phase modulator is shown in Fig. 3. To support wideband operation, two tunable integrators are implemented between the frequency divider the Gilbert-cell-based phase integrator. The slew-rate-control integrators assure that the I/Q triangle waveforms presented to the phase interpolator are of the same magnitude over the frequency of interest. The phase interpolator generates a carrier modulated with the desired phase, which is successively fed into the RF-DAC array whose 256 operating amplitude states are controlled by the AM decoder outputting 4 binary and 15 thermal bits.

The RF-DAC array are composed of inverse class-D switching power amplifiers [1], [2]. Thick-oxide devices are used for the top cascode devices to withstand the 2.5V supply voltage. The total size for the bottom cascode devices is 3 mm/65 nm. For the flip-chip assembly, the cascode drain connections are left open on the chip. The LTCC baluns on the two packages are designed with 2:1 turns ratio for the PA power delivery, and the drain supply is fed from the center tap of the LTCC balun.

The minimum spacing between the LTCC via pads limits the number of on-chip I/O pins. To address this problem, two differential 10:1 dual-edge-sampling deserializers are implemented to receive the amplitude and phase modulation



	R_P (•)	L_P (nH)	R_S (•)	L_S (nH)	K_M	C_B (pF)
LB	0.5	1.45	1.5	5.1	0.76	1.2
HB	0.37	1.08	1.5	3.0	0.76	0.82

Fig. 4. Transformer lumped model and the extracted parameters.

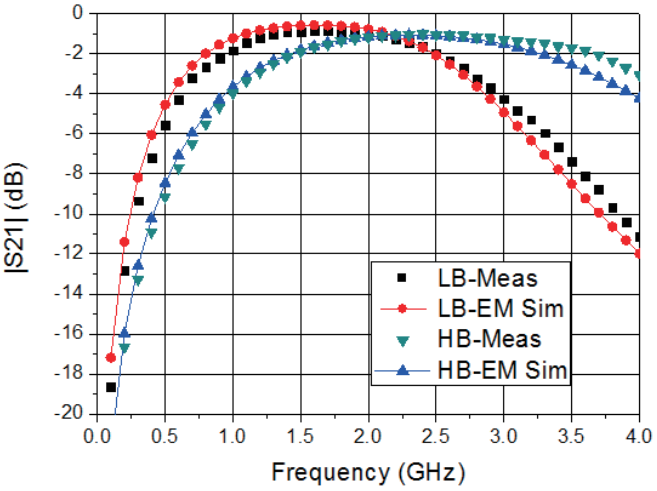


Fig. 5. Simulated and measured transformer performances on LTCC interposers.

codes respectively. The sampling (fast) clock runs at 1.25 GHz and the serial-to-parallel (slow) clock is at 250 MHz.

B. LTCC Interposer

The LTCC package is fabricated by VTT. The minimum dielectric thickness is 50 μm and the metal thickness is 10μm. The fine metal separation in vertical direction warrants the use of broadside magnetic coupling between metal layers; otherwise the magnetic coupling factors for broadband performance cannot be achieved. The two baluns on the LTCC packages have test structures which were individually measured by direct RF probing. The obtained 3-port *S*-parameters have been co-simulated with the rest of the circuit for better accuracy. Lumped models for the two baluns were created, and the model and the extracted parameters are shown in Fig. 4. Measurements show that the transformer quality factors are higher than 20 and Fig. 5 shows the measured and simulated insertion loss (S_{21}) of the LTCC baluns under differential to single-ended excitation. The load impedance is 50 • and the source impedance is 20 •, which is preferred by the PA. To estimate the minimum insertion loss and the frequency response, the results presented in Fig. 5 include two

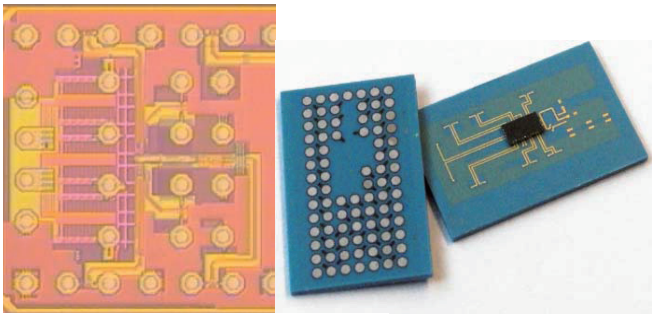


Fig. 6. Chip photo (with only the transmitter side included) and the package photo. The chip size is 1.8 mm^2 and the package size is about 1.5 cm^2.

ideal capacitors at both sides of the transformer windings, which in real case are realized by the device drain capacitance and the SMD capacitor on package. It is shown that the minimum insertion loss for both baluns are as low as 1 dB.

III. Transmitter Measurement Results

The chip and its package photo are shown in Fig. 6. The LTCC packages are connected to the PCB through a burn-in socket (Ironwood-6001). The two 2.5 Gb/s serial data streams are generated by the GTX transmitter from a Xilinx VC707 FPGA. The serial-link clocks and the LO signal are provided by CW signal generators. The output power is measured by a spectrum analyzer.

The measured peak power and the drain efficiency under 2.5V supply for the two packages for the two different frequency bands, low band (LB) and high band (HB) are shown in Fig. 7. The peak power/efficiency for the two packages are 27.1dBm/52% and 24.7dBm/40%, respectively. The measured power from 0.7 to 2.3 GHz is higher than 22 dBm with efficiency higher than 25%.

Fig. 8 shows the output amplitude with respect to the input AM codes with frequency at 1.2 GHz. Due to the code dependency on the switch resistance, the PA exhibits AM-AM and AM-PM distortion. Pre-distortion AM table containing information about the output magnitude and phase for each input AM code is applied to linearize the transmitter. AM-code-dependent I-R drop in the analog supply voltage degrades the transmitter linearity slightly.

The phase modulation is realized by selecting the proper PM code for the transmitting symbol with the AM-PM distortion taken into account. Fig. 9 shows the output phase to the different PM codes and the DNL for the phase response. Results from two frequencies, 1.2 and 2.5 GHz, are shown to verify the wideband operation of the proposed phase interpolator. The phase interpolator has a maximum DNL about 3º. The *S*-shape PM-PM curve is as expected since the output phase is synthesized by summing the I/Q quadrature currents. The weights of each current component are adjusted with the total weights fixed.

Digital modulations with 64 QAM, 802.11.ac (52 subcarrier OFDM, 54Mb/s) and LTE UL FDD (SC-FDMA, 63.4Mb/s) are tested and the results are summarized in Table I. The symbol mapping scheme for the tested 802.11.ac and LTE

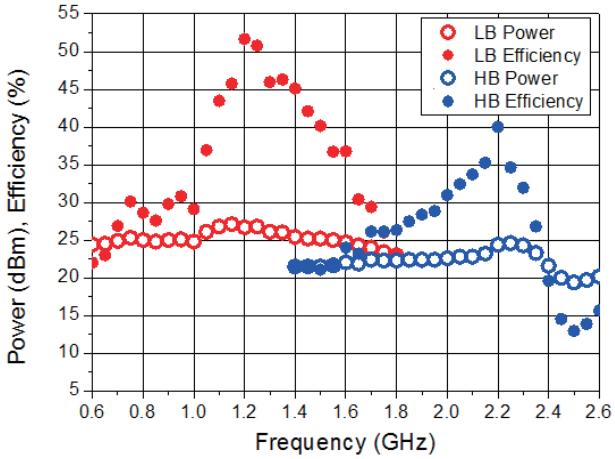


Fig. 7. Peak power and efficiency of the digital transmitter on the two LTCC packages. The low band (LB) covers 600MHz-1.7GHz, while the high band (HB) covers 1.6GHz-2.4GHz.

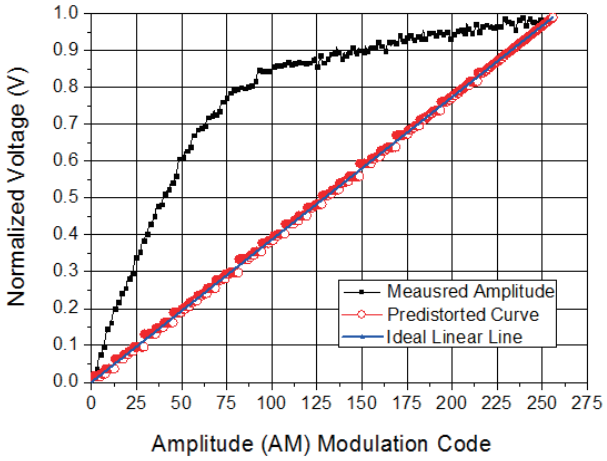


Fig. 8. Measured PA output amplitude to the amplitude codes (AM-AM) and the pre-distorted linear curve.

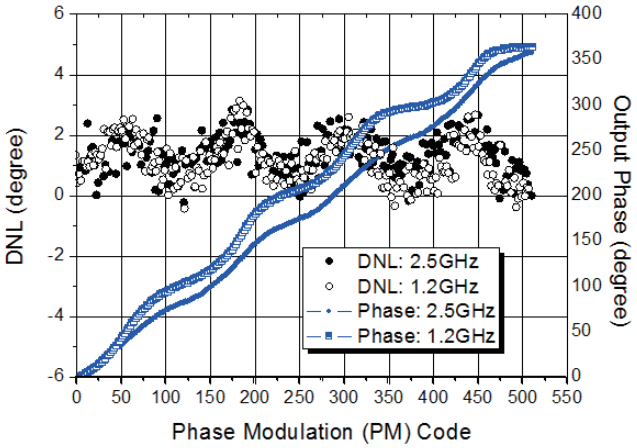


Fig. 9. Measured PA output phase to the phase codes and the phase deviation between consecutive phase codes.

TABLE I

TRANSMITTER PERFORMANCE UNDER DYNAMIC TESTING

Mod. Scheme	PAPR (dB)	Freq. (GHz)	Data Rate (Mb/s)	P_{AVG} /Eff. (dBm/%)	EVM (dB)
64 QAM	3.7	2.5	150	16.4/15	-25
64 QAM	3.7	1.2	150	20.0/29	-31
802.11.ac	8.0	1.2	54*	15.0/10	-26
802.11.ac	6.0	1.2	54*	18.4/16	-25
LTE UL	8.0	1.2	63.4*	16.7/12	-24
LTE UL	5.0	1.2	63.4*	19.2/17	-22

*Uncoded data rate

are both 64QAM and the measured EVM are -25 and -22 dB, respectively, with average output power about 19 dBm and efficiency about 17%. The measured LTE UL FDD is the touchstone where all the 100 resource blocks (RBs) and 1200 subcarriers are assigned to a single device (20-MHz bandwidth). The measured adjacent channel leakage ratios (UTRA-ACLR-1,2 and E-UTRA_ACLR) are below 36 dB with margin, which allows the use of external power amplifiers.

Table II compares this work with recently reported digital transmitters. Power and efficiency performance of this work is comparable to the highest reported values and the capability to support multiple RF frequencies is demonstrated.

IV. CONCLUSION

A high-power and high-efficiency CMOS digital transmitter incorporating the LTCC SIP technique is presented. The proposed PA generates 27.1 dBm output power and 52% drain efficiency under 2.5-V supply. Frequency reconfiguration is achieved by employing different LTCC interposers with flip-chip assembly. RF frequencies from 0.7 to 2.3 GHz is covered with output power higher than 22 dBm and efficiency higher than 25%. Digital modulations including 64QAM, 802.11.ac (WLAN OFDM), and LTE (SC-FDMA) are performed to verify the functionality of universal standard adaption.

TABLE II

PERFORMANCE OF CMOS DIGITAL TRANSMITTERS

Ref.	Architecture	Freq. (GHz)	P_{out} (dBm)	Eff. (%)	V_{DD} (V)
[1]	Polar	2.2	23.3	43	1.2
[2]	Cartesian	2.4	24.7	37	1.8
[3]	Polar*	2.25	25.2	45	3
[4]	Outphasing*	2.4	27.7	45	2.5
This Work	Polar	1.2	27.1	52	2.5
		2.2	24.7	40	2.5

*Off-chip phase modulator

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