A 0.4 GHz - 4 GHz Direct RF-to-Digital ΣΔ Multi-Mode Receiver

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***Abstract* — A wide-tuning-range low-power sigma-delta-based direct-RF-to-digital receiver architecture is implemented in 65 nm CMOS. A multi-level (two-bit) non-return-to-zero DAC improves jitter immunity to enable a high dynamic range, and, with a class-AB low-noise transconductance amplifier guarantees a highly linear front end. The peak SNDR of the receiver exceeds 68 dB for a 4 MHz signal, and is better than 60 dB across the 400 MHz to 4 GHz carrier frequency range. By virtue of utilizing a negative feedback digitizer close to the antenna, an IIP3 of +10 dBm and an IIP2 of +50 dBm is achieved while dissipating only 40 mW from 1.1 V / 1.5 V supply voltages.**

I. Introduction

Continued evolution of wideband wireless communications drives the need for flexible receivers capable of multi-mode, multi-standard operation. A universal 4G-LTE device, for example, is anticipated to operate from 450 MHz to 3800 MHz with varying bandwidth. A downconverting sigma-delta (ΣΔ) analog-to-digital converter (ADC) is an architecture capable of such operation [1], [2]. By embedding the mixer inside the feedback loop, a highly linear performance is achievable. By utilizing a low-noise transconductance amplifier (LNTA) in front of the ΣΔ ADC, this architecture can perform a lower noise direct RF-to-digital conversion. The center frequency is tuned by an external oscillator, and the bandwidth is set by the digital decimation filter. With high dynamic range, this architecture enables the ADC migrate closer to the antenna, enabling many signal conditioning features to be implemented in the digital domain, thus benefiting from technology scaling.

While the direct-conversion architecture is still prevalent in commercial mobile handsets, significant research efforts have shifted towards novel schemes that employ bandpass and downconverting ΣΔ ADCs. Previous implementations of downconverting ΣΔ receivers with switched-capacitor loop filters have demonstrated wide-tuning range or high dynamic range, but not both [2] [3]. In general, the dynamic range has been limited by the clock jitter injected from the feedback digital-to-analog converter (DAC). Jitter directly degrades the SNDR of the receiver, since it cannot be distinguished from input noise. A non-return-to-zero (NRZ) signal waveform helps reduce the jitter sensitivity by saving one of the transition edges, while a multi-level DAC improves the jitter immunity by reducing the amount of signal swing in each step. However, both techniques are challenging to implement at high frequencies. This paper demonstrates a system that achieves a high dynamic range together with a wide-tuning range, enabled by the implementation of a four-level NRZ DAC. The overall system linearity is further enhanced by a highly-linear class-AB LNTA input stage.

II. Receiver Architecture

The overall architecture of the receiver is shown in Fig. 1. It consists of both I and Q channels. An LNTA in each channel converts the input voltage into an output current. A programmable gain of 20 dB is implemented by changing the bias current in both the LNTA and the feedback DACs. The output of the LNTA is split into two interleaved paths for both I and Q channels, each of which contains a passive mixer, which is implemented as a sampling switch, followed by a passive switch-capacitor filter.

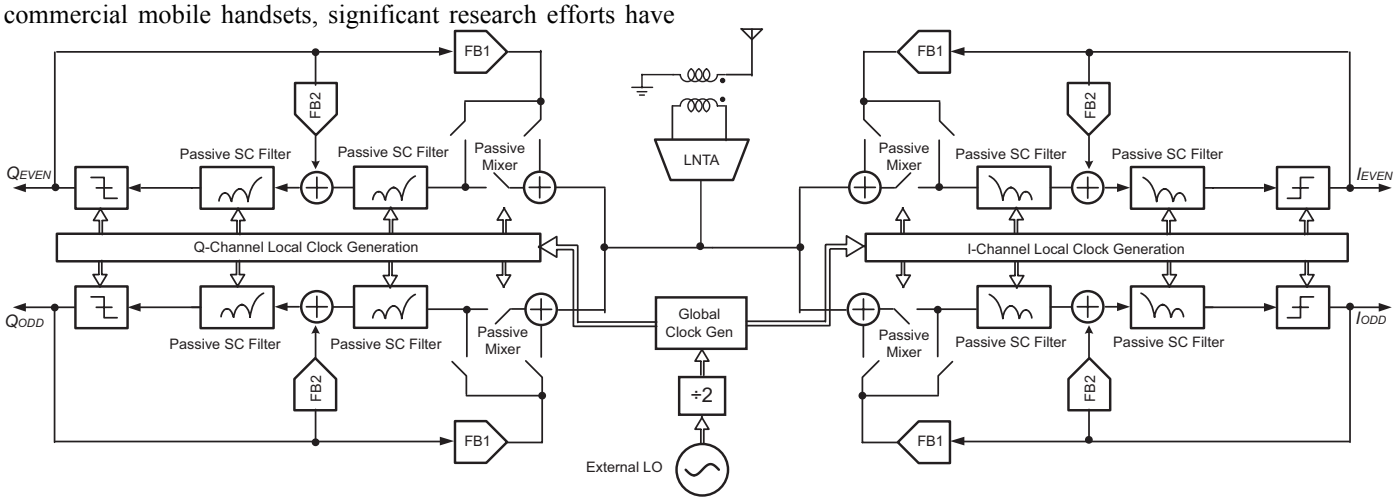


Fig. 1. Simplified block diagram of the receiver.

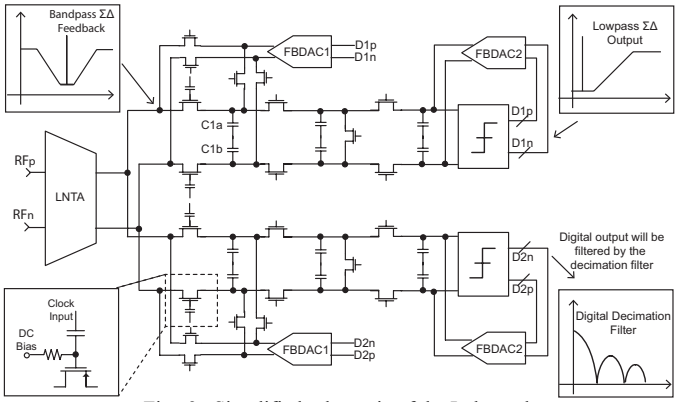


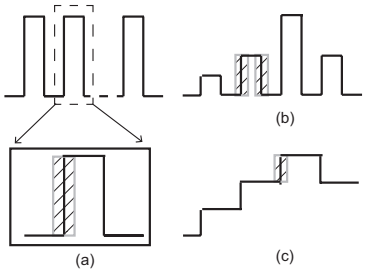
Fig. 2. Simplified schematic of the I-channel.

A detailed schematic of the I-channel is shown in Fig. 2. The high output impedance of the LNTA (~ 5 kΩ) forces the output current to flow through the mixer, switched at externally-supplied f_{LO}. When the LO signal is high, the output current from the LNTA charges a pair of capacitors (*C1a*, *C1b*) in the top path. When the LO signal is low, these capacitors are isolated from the input, and the signal is held constant. This two-path scheme indirectly implements a sample-and-hold function for the subsequent switched-capacitor circuits. The sampled-and-held signal is then processed by the second-order ΣΔ ADCs and is fed back to the output node of the LNTA. The sample-and-hold feature of the mixer limits the jitter sensitivity to the LO's edge rate only, however, the DAC implementation does impact the SNDR of the receiver.

III. Reducing the Impact of Jitter

The clock jitter from the first feedback DAC is a significant contributor to the overall noise budget in any high-speed ΣΔ modulator design. As illustrated in Fig. 3(a), the pulse duration of a return-to-zero (RZ) one-bit DAC varies from cycle to cycle, which is due to the clock jitter. As a result, the actual fed-back charge is modulated by the clock jitter and it causes the in-band noise floor to rise. There are two techniques that can reduce the impact of jitter: (1) increasing the number of levels in the feedback waveform, and (2) reducing the number of transition edges in the signal. With an increased number of levels in the RZ DAC, the amount of noise injected is reduced as the jitter is now only modulating the difference in the feedback levels, as illustrated in Fig. 3(b). An NRZ DAC can further reduce the effect of jitter, as shown in Fig. 3(c). The NRZ implementation reduces the number of transitions in the feedback waveform compared to the RZ implementation, since there are fewer opportunities for jitter to be added. Also, the wider pulse width in the NRZ waveform further alleviates the effect of jitter. The key challenge in designing an NRZ DAC at this speed is reducing inter-sample interference.

In this implementation, a four-level NRZ DAC has been selected to provide a theoretical 9.3 dB improvement in SNR over a two-level RZ implementation. A FIR-DAC-based multi-bit feedback scheme is attractive for ΣΔ ADCs, as the feedback can be created by an FIR filter and fewer comparators [4]. However, this approach is not suitable for a highly-linear receiver design because the FIR DAC's low-pass transfer function degrades out-of-band blocker resilience in the signal transfer function (STF).



Number of Levels	RZ DAC	NRZ DAC
2	Reference	0.6 dB
3	2.8 dB	5.9 dB
4	3.7 dB	9.3 dB
8	4.6 dB	17.1 dB
64	4.7 dB	36.3 dB

(d)

Fig. 3. Effect of clock jitter on RZ and NRZ DAC: a) illustration of the variation of clock pulse duration, b) RZ, c) NRZ, d) SNR improvement.

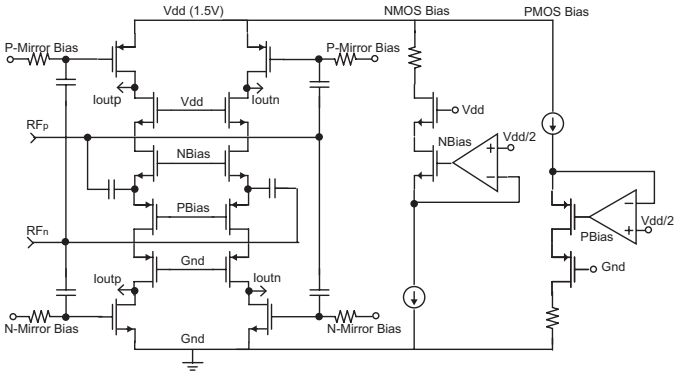


Fig. 4. Low-noise transconductance front-end with biasing.

IV. Circuit Implementation

A. Low Noise Transconductance Amplifier

Fig. 4 illustrates the schematic of the front-end LNTA. A class–AB dual common gate (CG) amplifier provides both wide band input matching and good linearity (i.e., +10 dBm). To improve the noise performance and the power efficiency, the g_m of the four tail current sources are reused by AC-coupling the RF input signal to their respective gates. The input common-mode voltage is set by two replica biases that mimic the biasing conditions of the NMOS CG and the PMOS CG. The LNTA's differential outputs are AC-coupled to the mixers (sampling switches), and the output common mode voltage is set by a common-mode feedback amplifier connected to the mixers. The LNTA provides a power gain of up to 20 dB from a 1.5 V supply. The key feature of this architecture is that the voltage swing at the LNTA's output is reduced by the loop gain of ΣΔ ADCs, thus improving the overall linearity performance of the system.

B. NRZ Feedback DAC

The two-bit NRZ DAC is implemented to favorably trade off jitter immunity with power consumption. The NRZ DAC, as shown in Fig. 5, operates in two phases, LO_D and $\overline{LO\_D}$, derived from the LO to reduce the inter-sample interference.

When the sampling (mixer) switches are closed, the feedback DAC is connected to the RF side of the mixer, suppressing the voltage swing at the LNTA and the sampling switches. During the second phase, the switches are open, and the DAC is connected to the baseband (*BB*) side of the switches, thus, preserving the DAC's NRZ feature. This scheme is sensitive to the clock jitter during the switching instances at the RF side only.

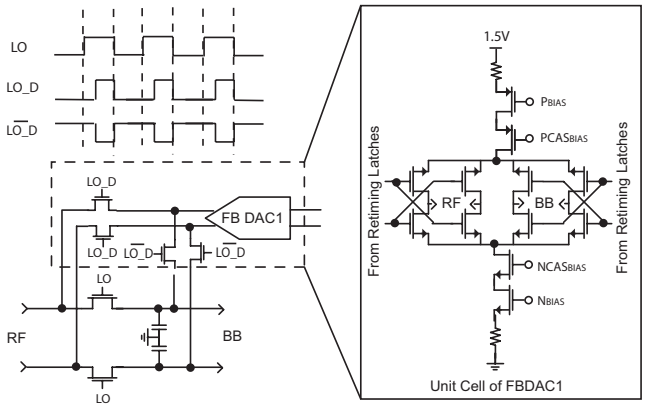


Fig. 5. Simplified schematic and clocking scheme for FBDAC1.

The DAC unit cell is shown in Fig. 5. To ensure voltage headroom for all the devices stacked in the unit cell and hence to maintain a high output impedance of the DAC (~10 kΩ), it is connected to the 1.5 V supply. Both the PMOS and NMOS current sources are degenerated for better matching performance. The DAC's switching signal is re-synchronized by a local latch within the FBDAC1 cell.

C. Other Circuits

The second feedback DAC design is less critical compared to the first feedback DAC, given that the jitter injected through that path is noise-shaped by the first integrator. Therefore, it is implemented as a simple RZ DAC.

The comparator, however, requires a short decision time (~200 ps), a small input-referred noise level (200 μV), and a low power consumption (4 mW at 2 GHz). The comparator core is implemented using a calibrated pre-amplifier followed by a sense-amplifier-based latch. The pre-amplifier helps to ease the stringent input-referred noise and mismatch requirements (0.5 mV) posed on the comparator, due to the lack of front-end gain in the system. The mismatch of the core comparators is further suppressed through an integrated calibration DAC to avoid using excessively large devices.

V. MEASURMENT RESULTS

The chip is implemented in a general-purpose 65 nm technology. The photomicrograph is shown in Fig. 6, highlighting that the receiver occupies an area of 850 μm × 650 μm, including the calibration DACs for the comparators as well as the local bypass capacitance.

Fig. 7 shows the measured SNDR for 4 MHz and 10 MHz signal bandwidths at 2 GHz. The peak SNDR is 68.86 dB for 4 MHz and 64.83 dB for 10 MHz, respectively. SNDR is higher than 60 dB over the 0.4 GHz to 4 GHz tuning range. Fig. 8 shows the SNR and SNDR for varying signal bandwidths at a 2 GHz center frequency. SNR and SNDR spectra are integrated from 10 KHz to the bandwidth of the system. Fig. 9 shows the output spectrum for a 2 GHz frequency with an input signal at 2.001 GHz. The low frequency spectrum is elevated due to the reciprocal mixing of the LO phase noise by the mixer.

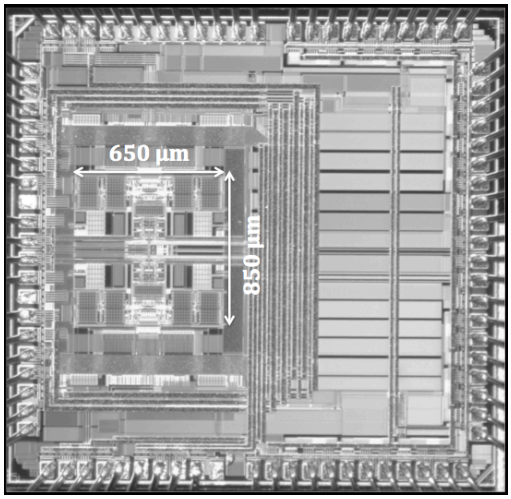


Fig. 6. Photomicrograph of the receiver.

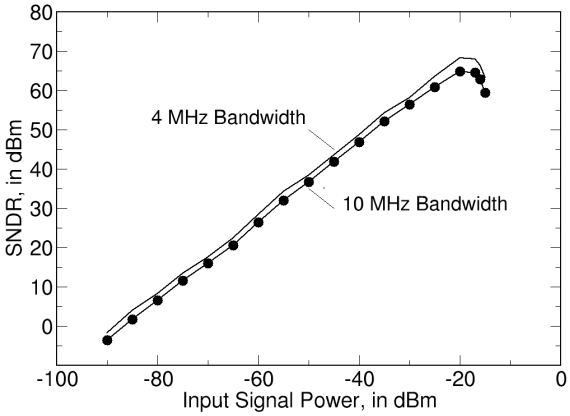


Fig. 7. Measured SNDR at 2 GHz carrier frequency.

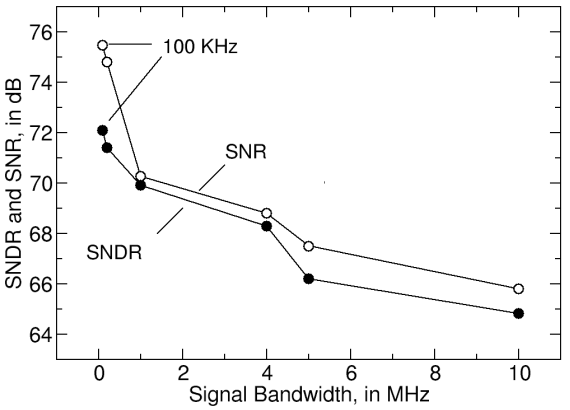


Fig. 8. Measured SNR and SNDR at 2 GHz carrier frequency.

Therefore, this receiver would achieve +10 dB SNR improvement for GSM, when operating in a low-IF mode.

Fig. 10 illustrates the IIP3 versus tone spacing. It demonstrates that the system maintains its high linearity over a wide range of blocker frequencies.

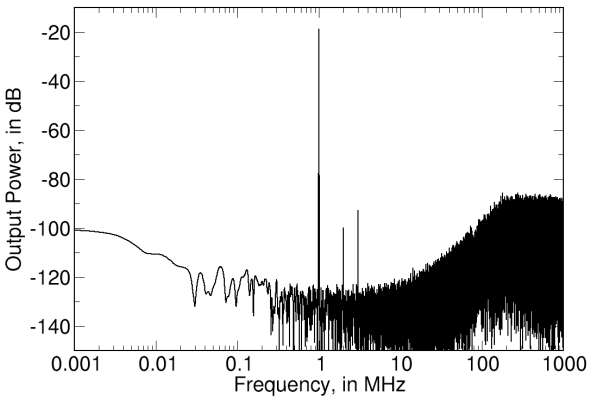


Fig. 9. Output spectrum at 2 GHz center frequency with input signal 1 MHz offset from the carrier.

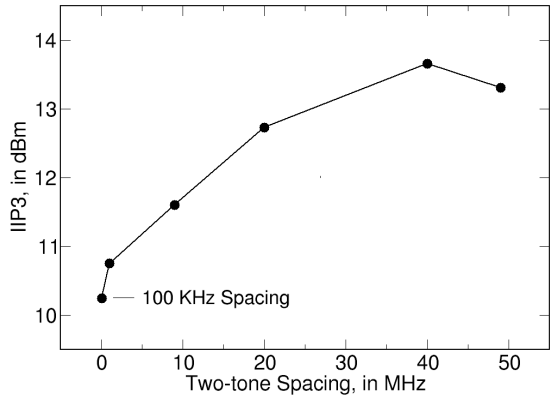


Fig. 10. IIP3 versus two-tone spacings at 2 GHz.

Fig. 11 shows the SNDR performance with the carrier frequency varied from 200 MHz to 4 GHz. The frequency resolution of the plot is limited by the sampling rate of the oscilliscope. At low frequencies, SNDR improves substantially with an increase in carrier frequency, as the in-band noise is dominated by the quantization noise. At higher frequencies, this improvement is offset by the increasing impact of the clock jitter. The clock jitter eventually dominates, so further oversampling only degrades SNDR. Table I lists the performance summary.

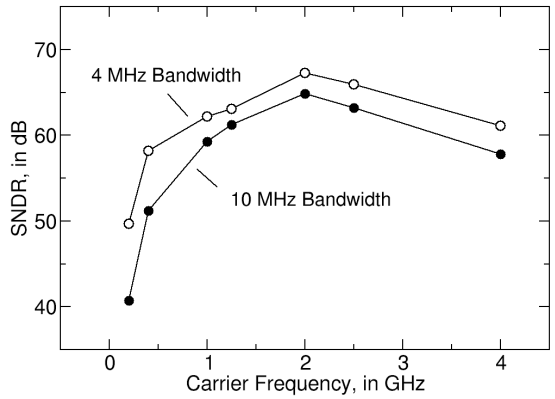


Fig. 11. SNDR versus carrier frequency.

TABLE I: RESULTS SUMMARY AND COMPARISON TABLE

Specifications	[6]	[2]	[5]	[7]	This work
Center Freq. (GHz)	0.8-2	0.4-1.7	0.4-6	0-1, 2-4	0.4-4
System	Bandpass ΣΔ	ΣΔ Modulator	RX AFE	Bandpass ΣΔ RX	RF-Digital ΣΔ
SNDR (dB)[1]	50-44	60	N/A	90 (SNR)	71-60
IB-IIP3 (dBm)	-5 / -7	+19	+6	+8	+10
OB-IIP3 (dBm)	N/A	+19	+10	+8	+13.5
IIP2 (dBm)	N/A	60	70	> 70	54-50
Sensitivity (dBm)[2]	-75[2]	N/A	3 dB NF	-97 7 dB NF	-88 16 dB NF
Power (mW)	30	50.4	30-55	1000	40.3[3] (17-70.5)
Area (mm^2)	2.3	0.8	2	5.5	0.56
Supply (V)	1.2	1.2	1.2	1.1 / 2.5	1.1 / 1.5
Technology	0.13 μm CMOS	90 nm CMOS	40 nm CMOS	65 nm CMOS	65 nm CMOS

[1] SNDR is measured for 1 MHz bandwidth
[2] Sensitivity is measured and reported for 10 MHz bandwidth except for [4], which is measured at 1 MHz bandwidth
[3] Power is measured at 2 GHz, including the divider power

VI. CONCLUSION

This paper presents a novel ΣΔ ADC based receiver that supports a frequency of operation from 400 MHz to 4000 MHz, which covers all LTE bands worldwide. An NRZ feedback DAC design reduces the jitter sensitivity of the system, and aids in achieving a high SNDR over the frequency range of interest.

ACKNOWLEDGMENTS

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