A 2.8GS/s 44.6mW Time-Interleaved ADC Achieving 50.9dB SNDR and 3dB Effective Resolution Bandwidth of 1.5GHz in 65nm CMOS

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Abstract

This paper presents a power- and area-efficient 24-way time-interleaved SAR ADC designed in 65nm CMOS. At 2.8GS/s sampling rate the ADC consumes 44.6mW of power from a 1.2V supply while achieving peak SNDR of 50.9dB and retaining SNDR higher than 48.2dB across the entire first Nyquist zone.

Introduction

High demand for low-power ADCs with sampling frequencies of 2-3GHz and effective resolution of 7-8 bits is driven by applications such as direct-sampling receivers in cable modems [1] and digital baseband implementations of 60GHz communication systems [2]. The state-of-the-art solution [1] consumes 0.48W of power and occupies an active area of 5.1mm^2. In this work both the area and power consumption of the ADC are each reduced by an order of magnitude. The main enabling technique for this improvement is miniaturization of the capacitors in the capacitive DAC of the interleaved SAR ADCs to the point where the ADC operates in a thermal noise limited regime. The minimum employed capacitor size is 50aF, ten times lower than previously reported [3] and well below the matching requirements, for a total sampling capacitance of 50fF and quantization noise at 10-bit level. This leads to a small area per channel and consequently allows for the distribution of input, clock, and reference signals without the need for power-hungry buffering. To be able to digitally correct static nonlinearities due to capacitor mismatches, a reduced radix of 1.85 is used in the capacitive DACs. A background least-mean-square (LMS) calibration technique that corrects static nonlinearities, offset, gain and timing mismatches has been implemented on the chip.

Chip Architecture

A high-level block diagram of the implemented ADC is shown in Fig. 1. It consists of M=24 time-interleaved channels, with two additional channels used for calibration. Each channel is split in two parts: analog (SARx_A, which also includes SAR logic), and digital (SARx_D). The digital part forms the final output by summing the weighted output bits from the analog part and the digital representation of the channel offsets. The values of digital weight coefficients and offsets are adaptive and are iteratively calculated in the 'linearity LMS' block. The timing LMS calculates timing mismatches and tunes the delay elements, Δt.

Two modes of conversion, named the direct and the reverse switching, can be selected in all channels. In the direct switching mode, after sampling the input signal onto all capacitors in the DAC, the MSB capacitor is connected to the positive reference V_{rp}, while all other capacitors are connected to the negative reference V_{rn} as shown in Fig. 2.a. In the reverse switching, the MSB capacitor is connected to V_{rn} and all others to V_{rp} (Fig. 2.c). After the first bit is resolved, the MSB capacitor is connected to V_{rp} if the resolved bit is '1' or to V_{rn} if the resolved bit is '0', both in direct and reverse switching (Fig. 2.b and 2.d). All other bits are resolved in a similar way. These two modes of operation have transfer characteristics that are 180° rotated with respect to each other, as illustrated in Fig. 3, for a 6-bit ADC with radix 1.8.

During calibration, two additional channels, SAR0 and SARt, sample the input signal together with one of the interleaved channels with sampling rate of $f_s/(M+1)$. The mode of operation is randomly chosen in SAR0 and SARt, while all interleaved channels perform direct switching. The difference between SAR0 output and the corresponding interleaved channel's output is an error signal (e) for the LMS algorithm, which calculates digital weight coefficients and offsets. The error signal is minimized when all transfer characteristics are equal and linear.

The timing calibration uses a coarse approximation of the input signal's derivative (D), obtained as a difference between the channels SAR0 and SARt, together with the error signal, e, to calculate the timing mismatches between channels as shown in Fig. 4. The bandwidth of the channel SARt is set to approximately one half of the bandwidth in other channels by placing a resistor in series with its inputs. Sign of e and sign of D with a dead-zone around zero are used both to improve convergence and to reduce hardware complexity. Final quantizer limits the resolution of the output control signal Δt_{dig} to 5 bits. The delays are implemented in the clock domain by inserting a variable capacitor C_{D2T} in the clock path as shown in Fig. 5. C_{D2T} are realized as a bank of small CMOS capacitors that are switched on or off to fine-tune the clock delays in steps of 300fs. After passing through the first-stage buffer, common for all channels, the main clock is gated by digital signals Φ_k in each channel to generate multiple clock phases. The sampling clocks drive the bottom-plate CMOS switches for improved resilience to the supply noise.

Measurement Results

The ADC is implemented in 65nm CMOS technology and consumes 44.6mW from a 1.2V supply when sampling the input signal at 2.8GS/s. For testing purposes an on-chip memory buffer is used to capture the 11-bit conversion outputs. SNDR degradation of less than 0.5dB is observed if final outputs are rounded to 10 bits. DFT plots before and after on-chip calibration for input signal close to the Nyquist frequency are shown in Fig. 6. After calibration, SNDR and SFDR are improved by more than 18dB. Fig. 7 shows performance plots for input frequencies up to 3GHz. The ADC achieves 50.9dB SNDR at low frequencies and retains SNDR higher than 48.2dB across the entire first Nyquist zone. Effective resolution bandwidth (ERBW) is 1.5GHz. SFDR higher than 55dB is maintained up to 2GHz. Energy per conversion is plotted in Fig. 8 together with prior-art ADCs with sampling speed higher than 1GS/s [4]. The standard figure of merit is 56fJ/conv-step with low frequency SNDR and 76fJ/conv-step with minimum SNDR in the first Nyquist zone. A die photo is shown in Fig. 9. The chip area including pads is 1.03 x 1.66 mm^2. The analog core area (all channels and clock generation) is 0.4 x 0.45 mm^2. Power consumption breakdown is shown in Fig. 10. Performance summary is in Table 1.

Acknowledgements

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References

[1] K. Doris, et al., IEEE ISSCC 2011
[2] IEEE 802.11ad PHY/MAC draft standard, IEEE 2010
[3] A. Shikata, et al., IEEE VLSI Circ. 2011
[4] B. Murmann, "ADC Performance Survey 1997-2011," [Online]

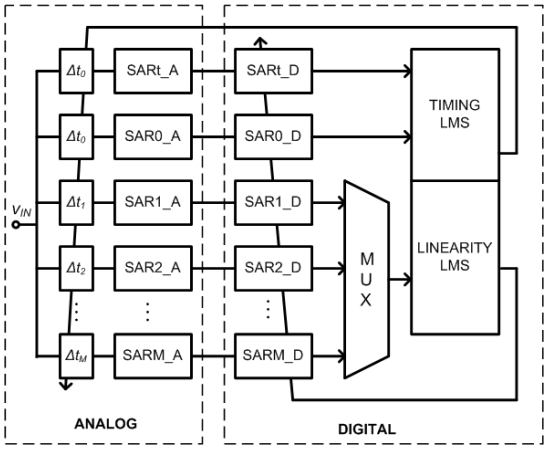

Fig. 1: Chip block diagram

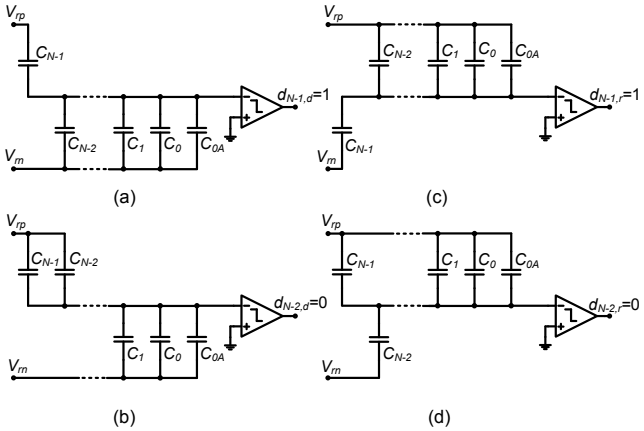

Fig. 2: Direct switching (a), (b), and reverse switching (c), (d)

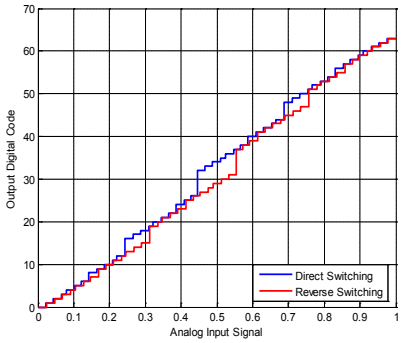

Fig. 3: Transfer characteristics for direct and reverse switching in radix-1.8 SAR ADC

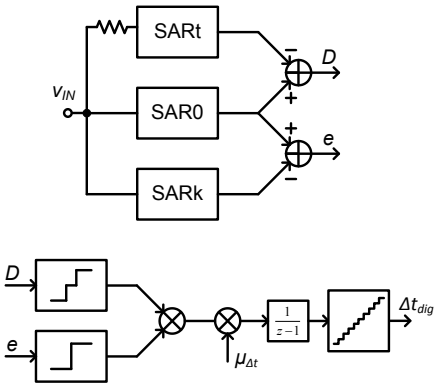

Fig. 4: Timing calibration block diagram

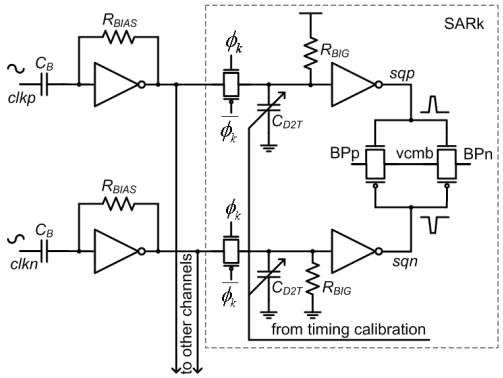

Fig. 5: Generation and tuning of sampling clocks

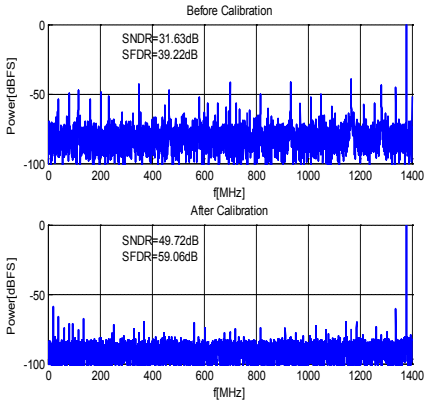

Fig. 6: DFT before and after calibration f_{in}=1379.56MHz

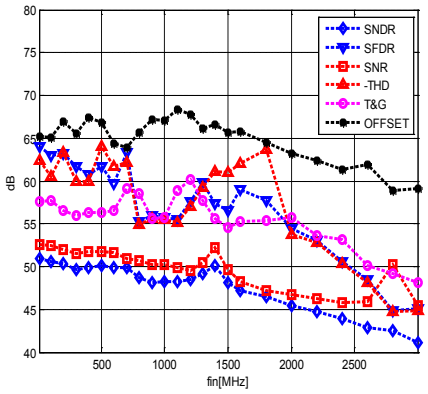

Fig. 7: Performance plots for input Frequencies up to 3GHz

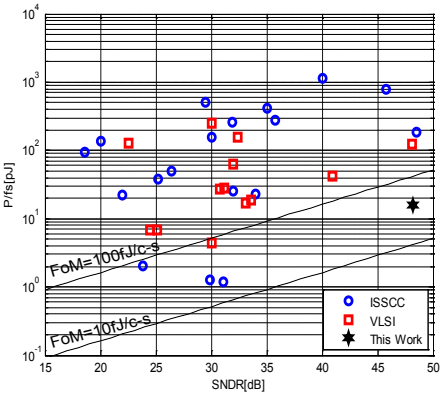

Fig. 8: Energy per conversion (ADCs with f_s>1GHz published at ISSCC and VLSI from 1997 to 2011)

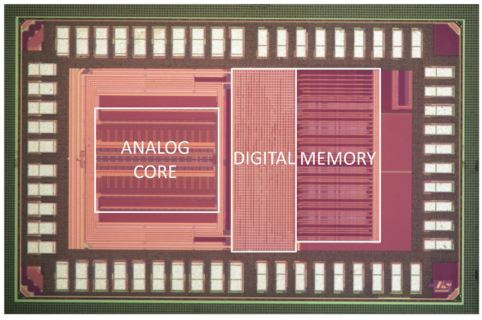

Fig. 9: Die photo
Analog core area: 0.4 x 0.45mm^2
Chip area: 1.03 x 1.66mm^2

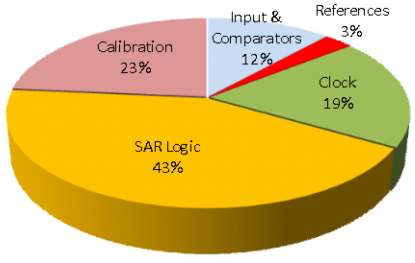

Fig. 10: Power consumption breakdown at f_s=2.8GHz, V_{dd}=1.2V

TABLE 1: Performance Summary

Sampling rate	2.8GS/s
Resolution	11b (10b with <0.5dB SNDR degradation)
Peak SNDR	50.9dB
SNDR	>48dB (up to 1.5GHz)
SFDR	>55dB (up to 2GHz)
ERBW	1.5GHz
Input bandwidth	>3GHz
Input	1.8$V_{pp\text{-}diff}$
Chip area	1.7mm^2
Analog core area	0.18mm^2
Technology	ST 65nm
Supply voltage	1.2 V
Power	44.6mW