6T SRAM Design for Wide Voltage Range in 28nm FDSOI

O. Thomas[1,2], B. Zimmer[2], B. Pelloux-Prayer[3], N. Planes[3], K-C. Akyel[3], L. Ciampolini[3], P. Flatresse[3] and B. Nikolić[2]
[1]CEA/LETI-MINATEC Campus Grenoble, [2]UC Berkeley-BWRC, [3]STMicroelectronics Crolles
Email: olivier.thomas@cea.fr, Tel: +1 (510) 229-9947

Abstract – Unique features of the 28nm ultra-thin body and buried oxide (UTBB) FDSOI technology enable the operation of SRAM in a wide voltage range. Minimum operating voltage limitations of a high-density (HD) 6-transistor (6T) SRAM can be overcome by using a single p-well (SPW) bitcell design in FDSOI. Transient simulations of dynamic failure metrics suggest that a HD 6T SPW array with 128 cells per bitline operates down to 0.65V in typical conditions with no assist techniques. In addition, a wide back-bias voltage range enables run-time tradeoffs between the low leakage current in the sleep mode and the short access time in the active mode, making it attractive for high-performance portable applications.

INTRODUCTION

The requirements for high performance and low power in portable devices highlight the need for circuit operation over a wide range of supply voltages (V_{DD}) to maximize energy-efficiency for a given performance requirement. However, increased variability in deeply scaled technologies prevents SRAM from achieving as low a $V_{DD,MIN}$ as logic [1]. Undoped thin-film planar FDSOI devices are being investigated as an alternative to bulk CMOS for the 28nm node and beyond because of their excellent short-channel electrostatic control, low leakage currents, and reduced random dopant fluctuations (RDF) [2,3]. This work investigates the design of a HD 6T SRAM array in UTBB FDSOI technology targeting wide voltage range. The key advantages include: (1) Back-plane (BP) doping underneath the buried oxide (BOX); (2) high body effect thanks to low SCE; (3) no dependency of the device functionality on the well doping type. (4) low V_T variability.

FDSOI TECHNOLOGY

In undoped-channel FDSOI technology, V_T is primarily set by the metal-gate (MG) stack work function. UTBB FDSOI offers additional flexibility by setting the BP doping type, either n or p. Combining BP and twin-MG process integration allows getting at least 3 distinct V_Ts (Fig. 1) [4]. In addition, the BOX dielectric electrically isolates the well from the source and drain of the transistors, which expands the range of possible well bias voltages (V_B) and therefore improves the range of possible V_T adjustments, through a high body factor. V_B is only limited by pn-well junctions. FDSOI achieves record low V_T variability because of its immunity to RDF even with forward body bias (FBB) [5].

METHODOLOGY

Analysis methodology in this paper is based on dynamic margins, obtained through transient simulations. Margins against read stability (RS), read access time (RA) and writeability (WA) failure are assessed using Monte Carlo (MC) based bit error rate (BER) estimates that do not make any assumption about the distribution of each failure metric, in contrast to other methods [6]. RS failures happen when the bitcell content flips accidentally or when the internal node voltage is less than 80% of V_{DD} at the end of the clock period during the read access. RA failures occur when the bitline difference voltage is less than the offset (100mV) of the sense amplifier at the end of the wordline (WL) pulse width. WA failures appear when the written internal node voltage is less than 80% of V_{DD} at the end of the clock period. The 80% threshold is considered to prevent bitcell failures on read access consecutive to any operation [7].

Importance sampling (IS) is used to speed up MC analysis of rare events [8]. The methodology used for this analysis finds the most probable failure point (MPFP) and samples around it to estimate the bit error rate (BER). Assuming that transistor V_T deviations can be modeled independently under a normal distribution, the MPFP is defined as the closest point to the origin in a multi-dimensional plot of V_T shifts [7]. Fig. 2 confirms IS correctly reproduces traditional MC results.

6T SPW BITCELL

For the analysis, the following conditions have been assumed: Typical process corner, 27°C, 28nm high density (HD) 6T bitcell with post-layout backend parasitic capacitances and a clock period scaling versus V_{DD} extracted on a critical path of an ARM 9 Cortex, assuming 2GHZ at 1V (25 standard cells loaded by neighbor + parasitic extraction). The bitcell initial condition is '1' and '0' on the left (L) and right (R) storage nodes, respectively (Fig. 3). The other bitcells in the column are biased complementary to set the column for the worst-case read condition. The simulations have been performed with a silicon-calibrated surface-potential based SPICE model [9].

For the bulk-like baseline bitcell (Fig. 3) $V_{DD,MIN}$ is limited by RA and WA (Fig. 4). In contrast to static analysis (with infinite access) RS margin, a dynamic metric, is high, even at very low V_{DD} thanks to the lack of time to flip the bitcell. For a distribution that exceeds 6σ in variation, $V_{DD,MIN}$ is 800mV for a 256b column tall. WA-limited $V_{DD,MIN}$ is 760mV.

The methodology not only estimates failure probability, but also tracks bitcell sensitivity to transistor strengths through evaluation of the MPFP. For a short clock period (CP), WA $V_{DD,MIN}$ is limited by the completion of the transition of the high logic level node driven by PMOS PU transistors (Fig. 5). For a slow CP, PG/PU current ratio causes the failure, which is typically considered in static analysis. RA limitation of the $V_{DD,MIN}$ is due to a low PG transistor drivability (Fig. 6). At high voltage (>0.7V), timing failures are caused by stability issues (PG_R is reinforced, while PD_R is weakened).

978-1-4673-2691-9/12/$31.00 ©2012 IEEE

To strengthen the PU, an SPW bitcell architecture is introduced, depicted in Fig. 7. Both PMOS and NMOS transistors are placed over a common P-well, which lowers the threshold of the PMOS transistors down to RVT value. The V_T of PD and PG NMOS transistors does not change, compared to the bulk-like bitcell. By increasing V_B, NMOS transistors are forward biased to improve RA and therefore $V_{DD,MIN}$. In this framework, the PW is isolated from the p-substrate by using a deep n-well (DNW) tied to V_{DDS}. Thanks to the single common well, V_B can be biased up to (or tied to) V_{DDS}, biasing the nMOS transistors in a full forward mode.

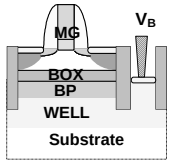
WA improvement lowers $V_{DD,MIN}$ by 120mV for 64 and 128 bitcell columns, while for 256b RA improvement lowers $V_{DD,MIN}$ by 60mV (Fig. 8). RS is also improved by almost one sigma due to the higher strength of the PU, which reinforces the high voltage level on the opposite side of the bitcell during the read stress (not represented in the paper).

The SPW architecture and V_B biasing improve $V_{DD,MIN}$ at the cost of increased leakage at same supply voltage. However, SPW bitcell leads to the best $V_{DD,MIN}$–leakage current tradeoffs (Fig. 9), in particular for a short bitline. For power management in a mobile processor, two back-bias modes can be considered. In active mode, V_B would be biased to V_{DD} to achieve the lowest $V_{DD,MIN}$ and in standby-mode V_B is grounded to minimize the static power, making the SPW bitcell compelling for high capacity cache designs.

CONCLUSION

The SPW 6T SRAM cell architecture lowers the $V_{DD,MIN}$ and offers an attractive option for a tradeoff between the leakage current and the access time through back biasing. Compared to the regular bitcell, the SPW bitcell achieves a $V_{DD,MIN}$ as low as 650mV, with no assist technique. Back biasing varies the leakage current between the active and standby modes, making it an attractive solution for high-density cache arrays in mobile processors. Finally, it is expected to reduce systematic variability components associated with well proximity effects due to the single well approach.

[1] E. Karl et al, ISSCC 2012. [2] K. Cheng et al., SOI conf., 2010. [3] N.Planes et al, VLSI'12 [4] J-P. Noel et al., TED, 2011. [5] O. Weber et al., IEDM 2010. [6] L. Ciampolini et al., JOLPE, 2012. [7] D.E. Khalil et al., VLSI, 2008 [8] L. Dolecek et al., ICCAD 2008. [9] O. Rozeau et al. SOI Conf., 2011.



nMOS	**n-MG**	**p-MG**
n-BP	RVT	SHVT
p-BP	HVT	-
pMOS	**n-MG**	**p-MG**
n-BP	-	HVT
p-BP	SHVT	RVT

Fig. 1: UTBB-FDSOI device cross sectional view. BP is electrically connected to VB through the well. The table summarizes V_T options based on BP and twin-MG process integration (R/H/SH: Regular/high/superHigh-V_T) [4].

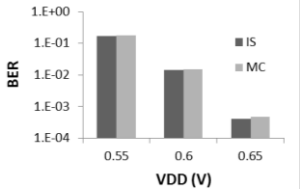


Fig. 2: Comparison of predicted writeability BER using both Monte Carlo (MC) and importance sampling (IS) for ρ< 0.1 [6]. BER smaller than 1^{E-4} cause an excessive MC runtime.

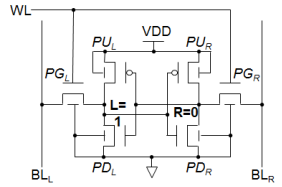


Fig. 3: Bulk 6T bitcell schematic. Left (L) side is holding 1 initially for read, write and retention analysis.

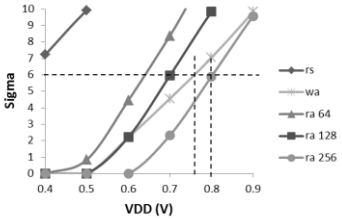


Fig. 4: Bulk-like 6T HD BER equivalent sigma vs. V_{DD} for read stability (RS), readability (RA) and writeability (WA) (TT, 27°C, 2GHZ@1V). RA was estimated for 64, 128 and 256 bitcells per column. WA $V_{DD,MIN}$=770mV; RA256 $V_{DD,MIN}$=800mV

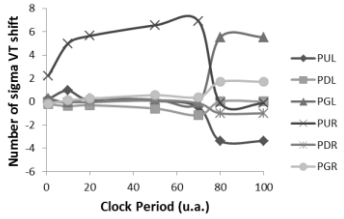


Fig. 5: Relative transistor strength impacting the WA BER vs. clock period (0.6V, TT, 27°C). At low frequency, PG/PU current ratio causes the failure rate, as usually reported in static write margin analysis. At high frequency the PU completion becomes the main cause of failures.

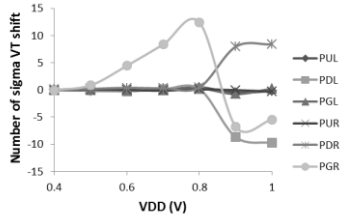


Fig. 6: Relative transistor strength impacting RA BER vs. V_{DD} (TT, 27°C, 2GHZ@1V, 64b). At low voltage, read time failure is mainly affected by PG transistor I_{ON} current. Above 0.7V, timing failures are caused by bitcell stability issues.

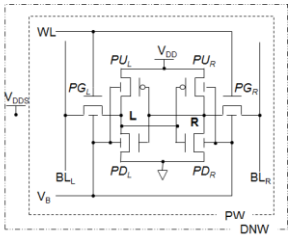


Fig. 7: UTBB-FDSOI 6T SPW SRAM bitcell schematic: PD & PG remain HVT, while PU transistors become natively RVT. V_B can be biased from a negative voltage up to V_{DDS}, the deep n-well (DNW) voltage.

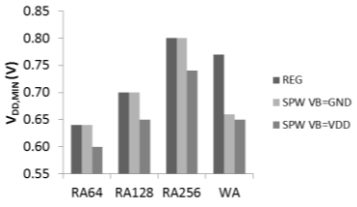


Fig. 8: $V_{DD,MIN}$ benchmark (TT, 27°C). SPW and V_B tied to V_{DD} leads to the lowest RA and WA $V_{DD,MIN}$. RA64/128 $V_{DD,MIN}$ < WA $V_{DD,MIN}$ = 650mV; RA256 $V_{DD,MIN}$ = 740mV.

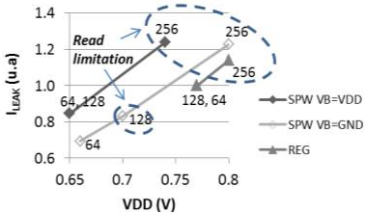


Fig. 9: Leakage current versus $V_{DD,MIN}$ for the various column tall (TT, 27°C). The results are normalized to the leakage current of the baseline bitcell extracted at $V_{DD,MIN}$ for a 64b column tall.