Planar Fully Depleted SOI Technology: the Convergence of High Performance and Low Power towards Multimedia Mobile Applications

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Abstract—**Planar fully-depleted SOI technology is becoming mainstream within STMicroelectronics, targeting modern mobile and consumer multimedia markets. This technology combines high performance and low power consumption, complemented by an excellent responsiveness to power management design techniques. The fabrication process is comparatively simple and is a low-risk evolutionary step from conventional planar bulk CMOS. At 28nm, we find that planar FD more than matches the peak performance of "G"-type bulk technology, at the cost and complexity of a low-power type technology, with better power efficiency across use cases than any of the conventional bulk CMOS flavors. FD implementation of a representative design offers 1.6x-7x speedup compared to bulk across a range of supply voltages.**

Index Terms—*28nm, FD-SOI, CMOS, high-performance, low-power, mobile, SoC, efficiency, Back-Bias, SPICE.*

I. INTRODUCTION

Driven by the strong growth of smartphone and tablet devices, an exponential growth for the mobile SoC market is forecasted up to 2016 and beyond. These systems, designed in the latest scaled technologies, require very high speeds to deliver a very high performance, while consuming remarkably low energy. However, designing such systems at the nanometer scale introduces many challenges due to the emphasis of parasitic phenomena driven by the scaling of bulk MOSFETs, making circuits more sensitive to the manufacturing process fluctuations and less energy efficient.

Traditional planar bulk CMOS technology has challenges to offer optimal performance for acceptable battery life in 28nm node. The two major detractors to the efficiency of traditional technology at these advanced nodes are the transistor variability and the electrostatics, which govern the on/off current ratios.

A. Transistor Variability

The root causes of variability in bulk CMOS technology are dominated by random dopant fluctuations (RDF) and line edge roughness (LER) [1]. These two sources of variability are not new, but their relative importance increases with technology scaling. The importance of RDF increases with the reduction in the number of dopant atoms in the channel. LER is a variation in gate patterning caused by the physical limitations of the lithography (resin, polymer size, wavelength). Both RDF and LER lead to a VT fluctuation; however, LER additionally increases subthreshold current due to short channel effects (SCEs).

A wide statistical distribution of VT affects the predictability of transistor behavior, where stability, performance, minimum operating voltage of SRAM are degraded, and total leakage of the chip increased, making it more difficult to sign-off designs in corner conditions.

B. Electrostatics

Due to the reduction of the spacing between the drain and the source with scaling, the gate switch efficiency of the devices is severely affected. The degradation of the ION/IOFF current ratio originates from SCE. The drain and source capacitances jeopardize the gate control over the channel, in particular with respect to the carriers distant from the Si-SiO_2 interface. SCE lead to an increased VT roll-off, which is reinforced by the drain-induced barrier lowering (DIBL). The non-gate controlled carriers increase the IOFF current, degrading the device subthreshold slope (SS) [2]. SS, SCE and DIBL degrade the leakage-performance trade-offs in circuits. In addition to the VT variability, they become a major concern for mobile and consumer multimedia applications, for which lowering Vdd is an important knob to reduce dynamic power.

The consensus workaround these issues is in thinning-down the silicon film of the devices in order to make ultra-shallow junctions and minimize the drain/source capacitance effect to get rid off non-controlled carriers away from the interface. Thin film transistors can be either planar or tri-dimensional. In the tri-dimensional flavor (FinFET or TriGate), the gate wraps around the sides of a vertical silicon 'fin'. In the planar flavor, thin film transistors are fabricated in an ultra-thin layer of silicon over a buried oxide (BOX) (Fig. 1). This is done by employing silicon-on-insulator (SOI) wafers as starting substrate, with an extremely thin top silicon layer. Thin film leads to fully-depleted transistors even when the transistor is in its off state. Since the channel is undoped, it solves many of the issues that conventional bulk CMOS faces. The gate retains excellent electrostatic control over the channel, achieving a DIBL lower than 100mV/V proven on silicon down to 18nm gate length [3] and record low variability [4] [5].

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II. TECHNOLOGY OVERVIEW

STMicroelectronics has chosen to implement planar fully depleted silicon-on-insulator ("planar FD", or equivalently "FDSOI") transistors that are planar CMOS transistors fabricated in a very thin layer of silicon sitting over a buried oxide (BOX). They are therefore 'ultra-thin body' (UTB) devices: the electrical conduction channel that forms between source and drain is confined into the ultra-thin silicon layer under the gate oxide (Fig. 1).

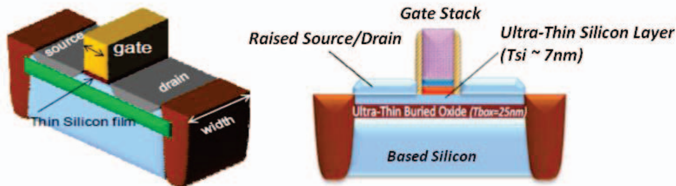

Figure 1. Planar FD device structure (notional perspective, TEM cross-section).

A. Ultra-Thin Buried Oxide

For the 28nm node, the selected BOX thickness is 25nm. It offers an excellent trade-off between drain/source-substrate parasitic capacitances and body factor. This ultra-thin BOX brings several other advantages:

- further improves the electrostatic control and relaxes the thinness requirement of the top silicon,
- enables back-biasing through the BOX,
- enables the implantation, during the fabrication process, of heavily doped "ground planes" or "back-planes" under the BOX, for improved electrostatics and/or VT adjustment and/or best-efficiency of back-bias,

In addition, the BOX offers total dielectric isolation of the very thin active layer and naturally ultra-shallow junctions, leading to lower source/drain capacitance, lower leakage and inherent latch-up immunity.

B. Immunity to Short channel Effects and Variability

Having a very thin body ensures all electrical paths between source and drain are very close to the gate, and the transistor regains excellent electrostatic control over the channel. As a result, sub-threshold slope, DIBL and other short channel effects are improved. In addition, the planar FD technology does not demand doping or pocket implants in the channel to control the electrostatic characteristics and tune the threshold voltages. Therefore, the major issue of random dopant fluctuation is reduced to the components stemming only from the source and drain regions. The absence of doping also helps performance, as the carrier mobility is not impeded by the dopants.

C. Multi-VT

While Multi-VT in planar bulk CMOS technology is implemented by multiple channel implant levels, this approach is not used in planar FD, which is essentially an undoped channel technology. In UTBB FDSOI technology, VT is set by the WELL doping type, either n or p.

Thanks to this, the 28nm FDSOI technology is capable of offering two VTs, RVT and LVT, for low-power and high-performance, respectively. In addition, some additional knobs are still available for reaching power consumption targets, including the gate length trimming (i.e. poly bias) and counter-doping.

D. Process Cost Considerations

The strategy when developing the 28nm planar FD technology has been to reuse as much as possible the 28nm low-power bulk CMOS process. Overall, the back-end of the line is identical to the traditional 28nm bulk low-power CMOS process, and the front-end is 80% common with that same process. In addition to sharing many steps, the planar FD process saves about 10% of the processing steps required to fabricate the chips. This roughly offsets the increased wafer cost. As a result, the 28nm planar FD technology matches the cost of a conventional low-power technology while, delivering extremely competitive performance.

III. CIRCUIT-LEVEL BENCHMARKING

To assess how the improved transistor characteristics translate at circuit level, several representative IP blocks, including an ARM Cortex-A9 CPU core were benchmarked using simulations with silicon extracted models. The following benchmarks compare the merits at the 28nm node of ST's planar FD technology ("28FD") with a state-of-the-art low-power technology ("28LP") and a more performance-oriented, state-of-the-art general purpose technology ("28G"). Competitive speed/leakage trade-off enables operation at reduced Vdd.

Figure [2] shows the competitive speed/leakage trade-off of planar FD vs. conventional bulk CMOS technologies at nominal voltage (0.85V for the G-type technology, 1V for 28FD and LP-type technology). For comparable leakage power, 28FD consistently outperforms both 28LP and 28G. In addition, applying forward back-bias (FBB) to the planar FD technology enables further pushing the performance, obviously at the expense of increased leakage, but without degrading the performance/leakage ratio (making this a possible solution for boosting the performance during short bursts).

Moreover, with 200mV Vdd underdrive, the 28FD may yield the same speed performance as 28LP with a reduced leakage. In addition, with adequate FBB, it is still possible to reach 2GHz operation in typical process conditions.

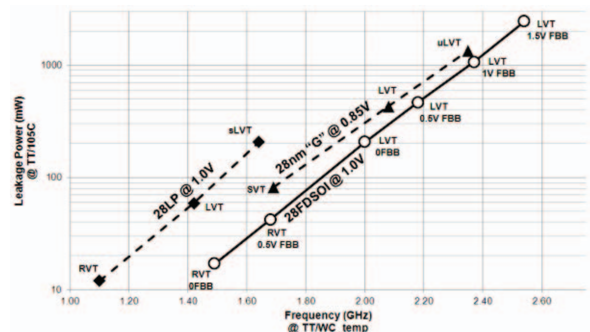

Figure 2. Best operating frequency for any class of leakage (worst-case process corner & temperature).

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A. *Best power efficiency across use cases*

Besides getting the best possible performance for a selected class of leakage, it is important to have access to the best possible total power consumption (dynamic power plus leakage power) across a wide range of operating frequencies.

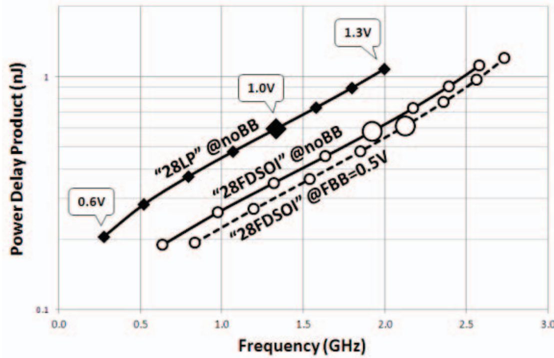

Figure 3. Compared PDP of LP and planar FD technologies (LVT flavor, typical corner, T=30°C)

In figure [3], the power-delay product (PDP) vs. frequency from 0.6 to 1.3V voltage range shows a speed increase from 30% to 150% without added energy cost. Moreover, FDSOI technology demonstrates attractive energy efficiency at same speed with a reduction of around 50% of power consumption at all voltages. We can also observe that 28LP is penalized by high dynamic power consumption (Vdd is higher), which negatively affects total power figures; in contrast, the 28FD technology is power-efficient across the full Vdd and target frequency range. In addition, with adequate forward body-bias (FBB) it is possible either to improve energy efficiency by playing with VDD/FBB trade-off or reach ultra-high speed for bursts of activity.

These observations are still valid at the ultra-low voltage (ULV) and even more attractive. In figure [4] power delay product (PDP) vs. frequency from 0.3 to 1V demonstrates very high speed gain on ULV profile. Frequency gain of FDSOI at fixed Vdd goes from 1.6X at 1V up to 7X at 0.3V. The relative reduction of energy over all voltage range is fairly constant, around 45% for RVT flavor. This is mainly due to the very good electrostatics of FDSOI devices boosting the effective current. For ULV design, we have the possibility to increase the gate length to reduce leakage current when aiming for low power. For example, using a 4nm-polybias reduces the leakage by 3X.

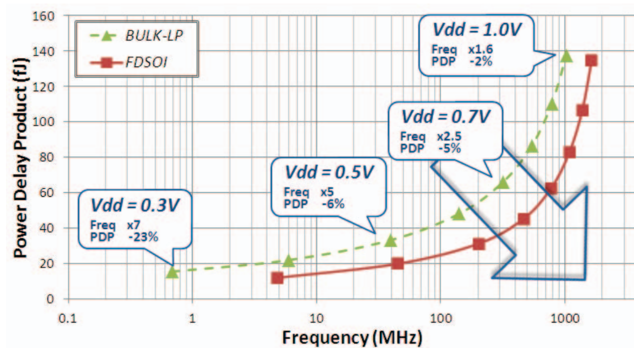

Figure 4. PDP simulations on Cortex-A9 critical path to ULV.

IV. Design Considerations

Designing on planar FD requires specific extraction deck and appropriate SPICE models. Apart from that, the design flows, methodologies and tools do not need any adaptation that would be specific to planar FD.

A. *SPICE Models*

Specific SPICE compact models have been developed for accurately representing planar FD transistors. For 28nm we are using the "UTSOI Spice Model" developed by LETI [6].

B. *Migration from Bulk (IP & SoC) at moderate effort*

A full design platform, based on the 28nm bulk has been developed for SOC applications. It contains standard cell libraries (multi-channel and multi-VT) with power management elements (power switches, level shifters etc.), embedded memories and analog IPs. It was derived from bulk by simple re-characterization of all the IPs over a wide range of back-biasing conditions. Only a limited number of critical IPs were tuned or redesigned: Analog IP, IOs and fuse. At SoC level, migrate an existing product from bulk to planar FD represents an effort comparable to a half-node migration.

C. *Power Management and Design Techniques*

All techniques used in low-power designs are applicable to planar FD. Especially, reverse & forward body-biasing and power switches can be enhanced with planar FD – keeping in mind that the voltage scaling is particularly efficient with FD.

Multi-VT

Although VT are set differently from bulk at the process level, this is transparent for designers. However, they get an additional possibility, if wished, to "program" VT by back-biasing: a continuum of VT values around the nominal value is available by modifying the back-bias voltage around its nominal value.

Power Switches

Power switches are an efficient leakage reduction technique, for low standby power consumption. Planar FD can exploit the back-bias capability to create efficient power switches. By implementing a hard gate-to-well connection, a 25% reduction of Ron is obtained. This results in a lower voltage drop across the switch in the on state, which can be exploited in two ways:

- for the same number of power switches around a given block, this block will see a higher effective supply voltage and run with better performance, or
- for the same voltage drop, fewer power switches need to be inserted, leading to area savings and a reduction of the leakage currents – we estimate that standby power can be reduced by over 25%.

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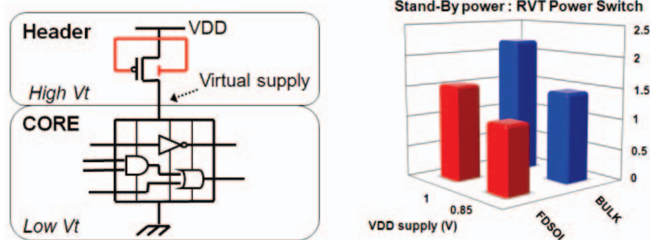

Figure 5. Planar FD optimized power switch.

BACK-BIAS

Back-biasing consists of applying a voltage just under the BOX of target transistors. Doing so changes the electrostatic control of the transistors and shifts their VT, to either get more drive current (hence higher performance) at the expense of increased leakage current or cut leakage current at the expense of reduced performance (Fig. 6).

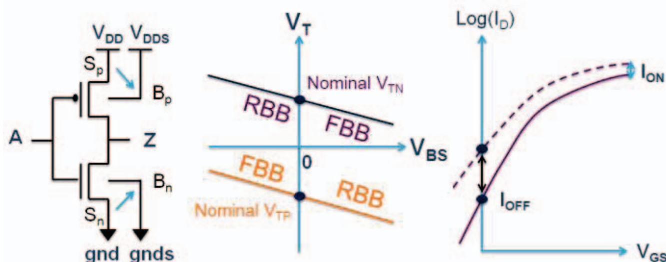

Figure 6. Back-biasing concept.

Back-biasing can be utilized in a dynamic way, on a block-by-block basis. It can be used to boost performance during the limited periods of time when maximum peak performance is required from that block. It can also be used to cut leakage during the periods of time when limited performance is not an issue. In other words, back-bias offers an efficient knob on the speed/power trade-off.

In bulk technology, body bias is rapidly losing efficiency as transistor dimensions shrinks; while back-bias in planar FD remains very effective thanks to better SCE. In addition, the maximum amplitude of the bias is limited with bulk CMOS, allowing only ±300mV range, otherwise leakage currents become unacceptable caused by the drain/source-substrate junctions. With planar FD, because the buried oxide the possible back-bias range is much wider, up to ±3V. So that, large performance boost factors can be obtained (Fig. 7).

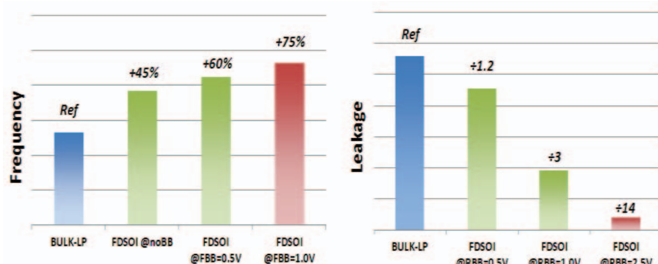

Figure 7. Performance boost with FBB and leakage reduction with RBB.

V. CONCLUSION

This paper presents a number of features that make planar FD is a promising technology for achieving high performance at low power consumption. Its remarkable performance and power are complemented by an excellent responsiveness to power management design techniques. The fabrication process is comparatively simple and is a low-risk, evolutionary step from conventional planar bulk CMOS – and there is little disruption at the design level. Planar FD more than matches the peak performance of "G"-type technology, at the cost and complexity of a low-power type technology, with better power efficiency across use cases than any of the conventional bulk CMOS flavor. FD SOI technology presents an attractive option for scaling for modern mobile and consumer multimedia applications to 20nm node.

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