Impact of Random Telegraph Signaling Noise on SRAM Stability

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Abstract

Large-signal bias and temperature dependences of random telegraph signaling (RTS) noise in transistors and their impact on the dynamic stability of 6T SRAM cells are investigated. RTS causes fluctuations in SRAM stability that are dependent on cell access history and trap characteristics. Access patterns for characterizing the worst-case and best-case dynamic stability are developed.

Introduction

RTS noise is projected to be a significant source of transistor variability, affecting the yield of highly scaled SRAM cells. Static SRAM margins, which correspond to infinite access time, traditionally have been used for estimating the impact of RTS on SRAM operation [1-2]. Predictions based on static margins are not accurate, however, because SRAM cells are always accessed dynamically with finite-duration word-line pulses [3]. Prior work quantified the effect of RTS on SRAM for fixed bias, ignoring the fact that the transistors within an SRAM cell undergo large-signal bias changes during actual operation that can affect trap occupancy characteristics [4]. In this work, the large-signal and temperature dependences of RTS and their impact on SRAM dynamic stability are investigated.

Transistor and SRAM RTS Characterization Setup

$0.252\mu m^2$ 6T SRAM arrays fabricated in a pre-production 45nm process (Poly-Si/SiO_xN_y gate stack) were used in this study. Large-signal and temperature dependences of RTS in individual transistors, as well as SRAM cell N-Curves, were extracted from a padded-out SRAM macro with full access to SRAM storage nodes (macro A) [1]. SRAM dynamic stability was measured from a separate set of SRAM cells (macro B) using an on-chip pulse generator [3]. RTS in the individual SRAM transistors in macro B was characterized through direct bit-line current measurements [5].

Large-Signal and Temperature Dependence of RTS

Large-signal RTS characteristics are studied by pulsing the gate voltage to V_{init} for 1s prior to drain current measurement at 0.7V (Fig. 1), to emulate the biasing of SRAM transistors during dynamic operation [1]. This process is repeated 50 times to obtain the average drain current. Fig. 2(a) plots the resulting single-measurement and average drain currents. α is defined as the trap occupancy probability. Analysis of the average trace shows that the trap is initially occupied (α=100%, low current) and that α exponentially decays to a new level with a characteristic time constant that is strongly temperature dependent (Fig. 2(b)). Fig. 3 plots the results (obtained with a different transistor) for V_{init}=0.0V. In this case, α is initially 0% due to the off-state pre-bias condition, and it eventually transitions to 100% with a characteristic time constant that is also strongly dependent on temperature. A few devices were observed to exhibit an opposite pre-bias voltage dependence, *i.e.* V_{init}=1.0V results in α=0% initially. The bias and temperature dependences for these devices (ref. Fig. 4) are indicative of type-II traps [6].

These results demonstrate that, although a trap might not be active at a certain bias condition, it can still affect SRAM operation because the characteristic time constant is significant for typical SRAM operating frequencies. Furthermore, the temperature dependence of RTS causes traps to appear as RTS in SRAM margins at high temperatures and as fixed traps at lower temperatures. This is evident from the high-speed sweeps of SRAM N-Curve write margins plotted in Fig. 5.

SRAM Dynamic Stability

Dynamic stability is defined as the critical word-line pulse-width for successful read/write operation [7]. The circuit schematics in Figs. 6 and 7 illustrate the biasing of SRAM cells under read and write access, respectively. SRAM cells in macro B were accessed using various large-signal biasing patterns (Fig. 15) to evaluate their impact on dynamic stability. T_{access} and T_{write} were swept to collect statistics on read and write success as a function of pulse width. Specific cells, with RTS identified only in a single transistor, were selected to study the impact of RTS in a specific transistor on dynamic stability.

Fig. 8 shows the trap occupancy behavior for transistor *PD1* and its effect on SRAM read access time. The bias conditions prior to read access (ref. Fig. 6) force trap occupancy in *PD1* which degrades T_{access}. This results in T_{access} that is dependent on the delay since the last write operation (T_{relax} in Fig. 15), as shown in Fig. 9. (T_{relax} needs to be shorter than the characteristic time constant of the traps to observe this dependence.) Read-after-write access was observed to be faster than single-read access because the detrimental bias condition is only applied for a short 200ns period. The opposite trend is observed in a different cell with a type-II trap in *PD1*, due to the opposite gate-bias dependence of type-II traps (Fig. 10).

Figs. 11 and 12 show the trap occupancy behaviors for each trap type in transistor *PU2* and their effects on SRAM write access time. The bias conditions prior to write operation (ref. Fig. 7) either improve or degrade T_{write} depending on the trap type. (Write-after-write access is relevant to SRAM performance because the 200ns delay between writes amounts to a few hundred CPU cycles.)

Since transistor *PU1* pulls node *CL* up to V_{DD} to complete the write operation, RTS in *PU1* can also impact write access time, as shown in Fig. 13. Finally, although the *PG* transistors are only turned on for a short duration during SRAM cell access, sequential pulses on *PG1* during read-after-read access are sufficient to force trap occupancy in *PG1* and degrade T_{access} of the final operation (ref. Fig. 14).

Figs. 16 and 17 plot the fluctuations in T_{access} and T_{write} (referenced to their nominal values) *vs.* nominal value. Positive and negative fluctuations are observed indicating that both conventional and type-II traps contribute to variability in SRAM dynamic stability. Similarly as for static margins [1], nominally weak cells (long access times) exhibit smaller RTS.

Conclusion

Low-frequency RTS causes fluctuation in SRAM dynamic stability. This needs to be factored into SRAM built-in-self-test design and statistical analysis, by considering the worst-case combinations of trap occupancy for read and write access. Worst-case fluctuations are determined by comparing the cases of single-access *vs.* multiple-access with minimum delay between operations. Although RTS can cause up to 45% fluctuation in strong cells, SRAM dynamic stability is still dominated by nominally weak cells with small RTS.

References

[1] S.O. Toh *et al*., *IEDM Tech. Dig*., pp. 767-770, 2009.
[2] M. Tanizawa *et al*., *Symp. VLSI Tech.*, pp. 95-96, 2010.
[3] S.O. Toh *et al*., *Symp. VLSI Circ.*, pp. 35-36, 2010.
[4] H. Miki *et al*., *IEDM Tech. Dig*., pp. 620-623, 2010.
[5] X. Deng *et al*., *Symp. VLSI Circ*., pp. 44-45, 2008.
[6] T. Nagumo *et al*., *IEDM Tech. Dig*., pp. 628-631, 2010.
[7] D. Khalil *et al*., *IEEE Tran. VLSI Systems*, pp. 1639-1647, 2008.

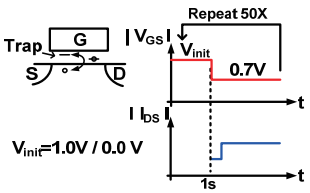

Figure 1 – Waveforms for alternating-bias large-signal trap response characterization.

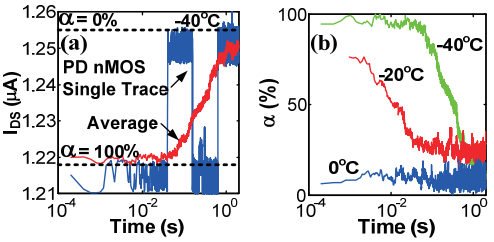

Figure 2 – (a) Drain currents extracted using alternating-bias with V_{init}=1.0V (b) Temperature dependence of trap occupancy.

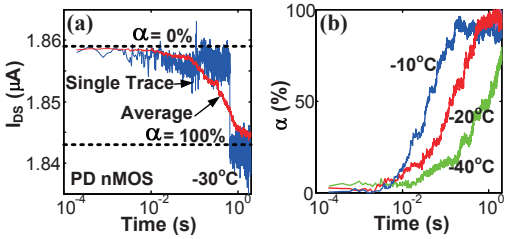

Figure 3 – (a) Drain currents extracted using alternating-bias with V_{init}=0.0V (b) Temperature dependence of trap occupancy.

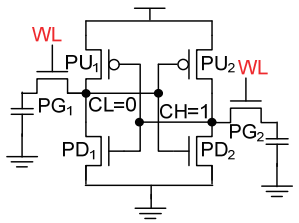

Figure 6 – SRAM schematic for read access. Internal node *CL* stores a "0".

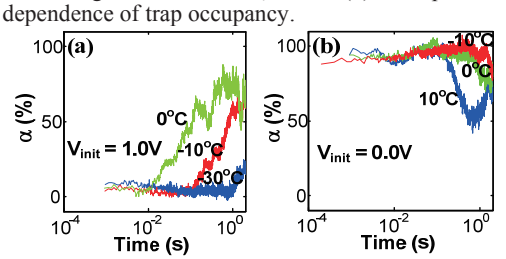

Figure 4 – Trap occupancy temperature dependence of type-II RTS with (a) V_{init} = 1.0V (b) V_{init} = 0.0V.

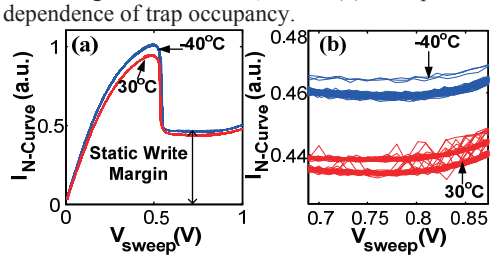

Figure 5 – (a) High-speed N-Curve sweeps of SRAM write margin at two temperatures (b) Zoomed-in view of region defining static SRAM write margin.

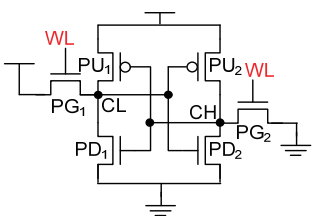

Figure 7 – SRAM schematic for writing a "0" into node *CH*.

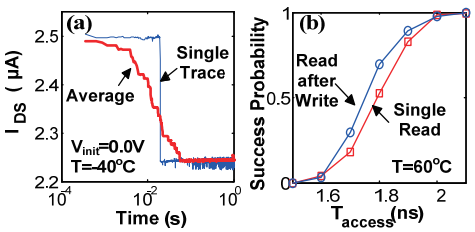

Figure 8 – (a) Large-signal occupancy of a trap in *PD1* (b) Statistical distributions of T_{access} for single-read and read-after-write.

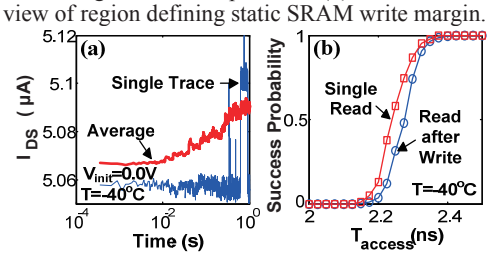

Figure 10 – (a) Large-signal occupancy of a type-II trap in *PD1* (b) Statistical distributions of T_{access} for single-read and read-after-write.

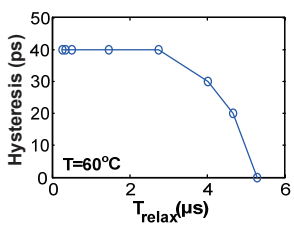

Figure 9 – Dependence of T_{access} fluctuation on delay since last write access (T_{relax}).

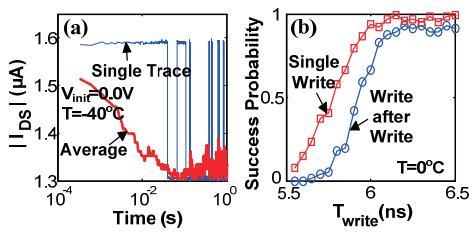

Figure 11 – (a) Large-signal occupancy of a trap in *PU2* (b) Statistical distributions of T_{write} for single-write and write-after-write

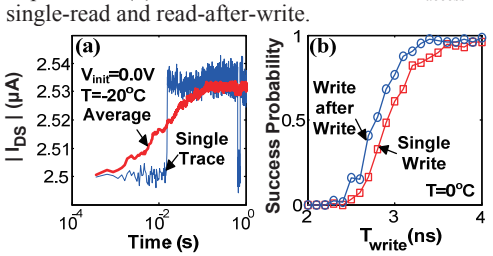

Figure 12 – (a) Large-signal occupancy of a type-II trap in *PU2* (b) Statistical distributions of T_{write} for single-write and write-after-write.

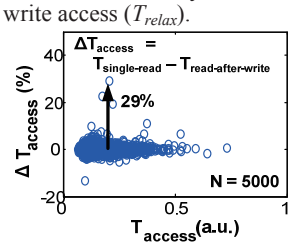

Figure 16 – Scatter plot of ΔT_{access} due to RTS vs. nominal T_{access}.

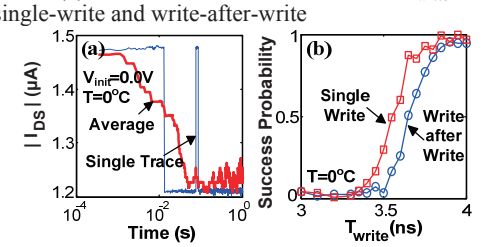

Figure 13 – (a) Large-signal occupancy of a trap in *PU1* (b) Statistical distributions of T_{write} for single-write and write-after-write.

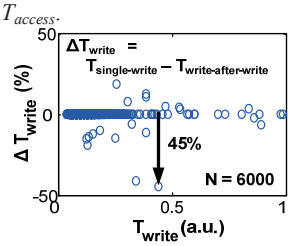

Figure 17 – Scatter plot of ΔT_{write} due to RTS vs. nominal T_{write}.

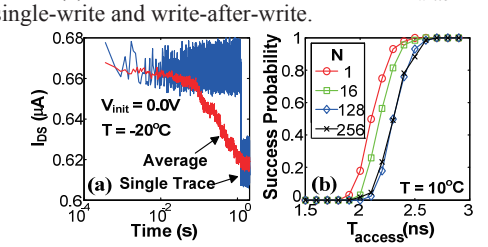

Figure 14 – (a) Large-signal occupancy of a trap in *PG1*. (b) Statistical distributions of T_{access} with *N* read-after-read cycles, saturating at *N*=128.

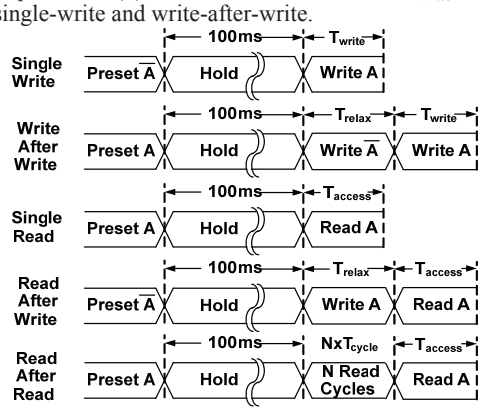

Figure 15 – SRAM access patterns for evaluating the impact of RTS on dynamic read and write stability. T_{relax} = 200ns to maximize fluctuations.

Acknowledgements: STMicroelectronics for chip fabrication. This work was supported by the Center for Circuit & System Solutions (C2S2) Focus Center, one of six research centers funded under the Focus Center Research Program, a Semiconductor Research Corporation program.