Dynamic SRAM Stability Characterization in 45nm CMOS

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Abstract

A method for characterizing dynamic SRAM stability using pulsed wordlines, is demonstrated in 45nm CMOS. Static read margins were observed to overestimate failures by up to 1000x while static write margins failed to predict outliers in dynamic write stability. Dynamic write stability was demonstrated to exhibit an enhanced sensitivity to process variations, and negative bias temperature instability (NBTI), compared to static write margins.

Introduction

Static (DC) noise margins are often used to characterize SRAM because of their simple interpretation and measurements, although they overestimate read failures and underestimate write failures. Alternately, dynamic SRAM stability has been proposed to be characterized by using critical wordline pulse width, which produces better estimates of failure rates [1-3], but this method has not been compared with static margins. This work demonstrates the on-chip circuitry for characterizing dynamic SRAM stability using wordline pulses with accuracy better than 10ps.

Dynamic Stability Characterization Circuits

Fig. 1 shows the SRAM array configuration for the characterization of the dynamic metrics and the necessary infrastructure for collecting static metrics for the purpose of establishing correlations between the measured results. A pulse of programmable width is generated centrally and delivered to a wordline following the row decoders. To avoid process- and layout-induced uncertainties, the exact pulse width is measured by wordline samplers located on every wordline. Each sampler consists of a high bandwidth dual-phase-clocked track-and-hold circuit followed by a comparator with offset calibration. The use of dual-phase-clocked track-and-hold circuits as well as calibration of the phase of these dual-phase clocks is essential for sampling the fast rising and falling transitions of wordline pulses with minimal distortion. This calibration scheme produces finer resolution compared to delay-line based schemes [4]. All array bitlines are accessible externally through a bitline switch network using 4-terminal Kelvin sensing to bias the bitline voltages during dynamic stability measurements as well as to characterize static read and write SRAM metrics [5].

Fig. 2 illustrates key circuit blocks for enabling accurate on-chip pulse generation. Two clock signals with a slight difference in clock period (ΔT) are used to produce a pulse train with a pulse width difference of ΔT between successive pulses. A counter is then used to select the desired pulse, based on a programmed digital codeword. This counter is synchronized by a *sync* signal which is asserted when Φ_0 and Φ_1 have the desired phase relationship. Phase calibration of the sampling edges of the wordline samplers is accomplished by capacitively summing both sampling edges and adjusting the skew between them to reduce the glitch on the summing node. A Monte Carlo simulation of this scheme reveals that it reduces the phase offset of respective edges to less than 3 ps. The impact of clock jitter on measurement accuracy is reduced through averaging. The built-in-self-test (BIST) circuitry also implements a pulsed-read mode for reading the contents of the SRAM cell at low supply voltages without disrupting the cell. In this mode, a programmable number of short pulses is applied on the wordline to develop enough differential bitline voltage before the sense-amplifier is enabled. This mode allows testing of the SRAM cell without the need of setting the supply voltage to a higher level for read-back.

Implementation and Results

The methodology was validated in a 45nm 7M1P CMOS process. Fig. 3 shows the die photo of the fabricated test chip. Two arrays were configured with 64 columns to minimize wordline pulse distortion due to parasitics. Such distortions will introduce a column dependent systematic error in the characterization of dynamic metrics. Fig. 4(a) verifies the functionality of the pulse generator by plotting the subsampled wordline pulses from the SRAM array in the equivalent time. The pulse generator produces programmable pulses with approximately 75ps rise times and 30ps fall times at the end of the wordlines. Fig. 4(b) plots the transfer function between the programmed codeword and actual pulse width. This transfer function is inherently monotonic, due to the pulse generation scheme, which allows the use of efficient binary-search-based BIST circuitry. Calibration of the pulse generator is not required if a 100ps error is tolerable. The wordline samplers were used to characterize the non-linearity of every wordline in order to achieve 10ps pulse width accuracy.

Fig. 5 compares the fail bit count between DC and dynamic conditions demonstrating the optimism of DC write margins and pessimism (up to 1000x) of DC read margins compared to dynamic stability. Fig. 6 plots normalized read access time against static read current (I_{read}). Measurements indicate good correlation with I_{read} after results are normalized with sense-amplifier offset voltages and bitline capacitance using the equation listed in Fig. 6. Fig. 7 plots statistical distributions of dynamic read stability [2]. The SRAM cells are biased with extra read stress, as indicated in Fig. 7, because the cells are extremely stable under nominal conditions (Fig. 5). Dynamic read stability with read-after-read operation is measured by configuring the pulse generator to deliver multiple pulses. Read-after-read operation, under extra read stress conditions, is observed to degrade dynamic stability by 1ns, or 10%.

Fig. 8 plots the correlation between dynamic write stability [2] and static bitline write margin (BLWM) [5] for 1024 cells. Correlation between dynamic and static write margin is only observed at $V_{DD,low}$ (Fig. 9a). Outliers in the dynamic write stability exceed cells which are in good correlation with the corresponding static write margin by more than an order of magnitude. These outliers correspond to the cells that have strong write margins at the opposite side of the cell (Fig. 9b). Sensitivity analysis in Table I indicates that dynamic write stability is strongly dependent on the PMOS of the opposite side (PU2) making it more susceptible to asymmetry, random telegraph signals (RTS), and NBTI, compared to static margins. Fig. 10 plots measurements of dynamic write stability before and after NBTI stress, indicating both degradation (up to 2X) and improvement in write stability, contrary to predictions that write stability is only improved by NBTI [6].

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References

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[4] R. Joshi, et al., VLSI Circ., 2007.
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[6] S. Kumar, C. Kim, and S. Sapatnekar, ISQED 2006.

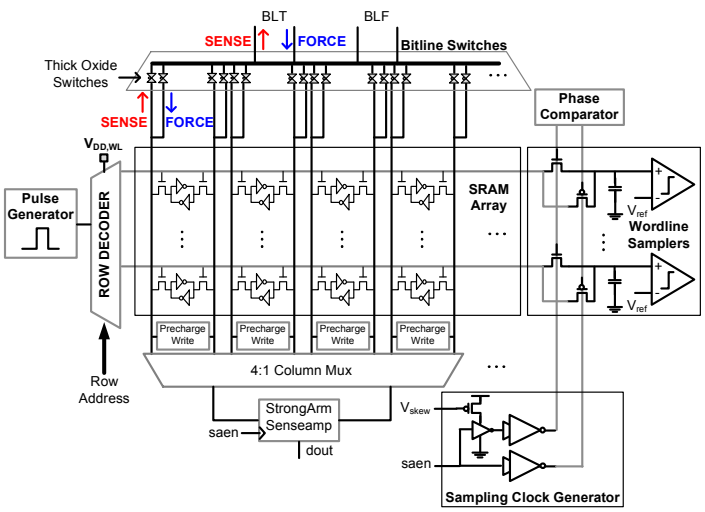


Figure 1 – SRAM array block diagram.

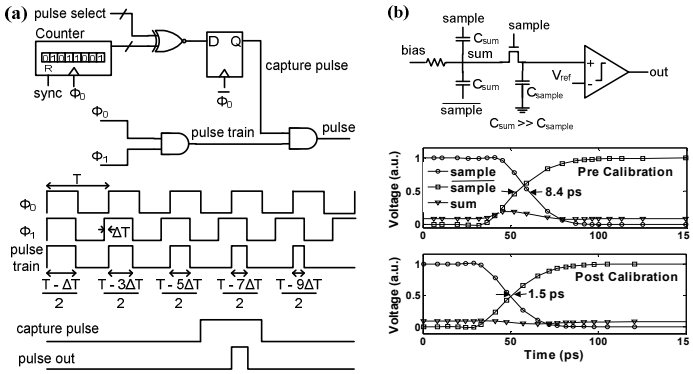
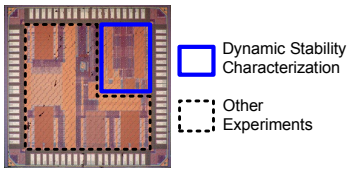


Figure 2 – Schematic of (a) pulse generator and (b) phase comparator with simulated waveforms.



Technology	ST 45 nm 7M1P CMOS
SRAM Bit-cell	6T 0.252 μm^2
Pulse Accuracy	10 ps
Pulse Resolution	1 ps
Chip Dimensions	1.55 mm x 1.55 mm

BLS : bitline switches
WLS : wordline samplers
LS+WLD : level shifters & wordline drivers.
CIO : column I/O circuitry

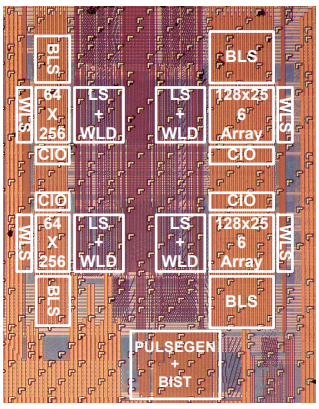


Figure 3 – Die photo and table of specifications.

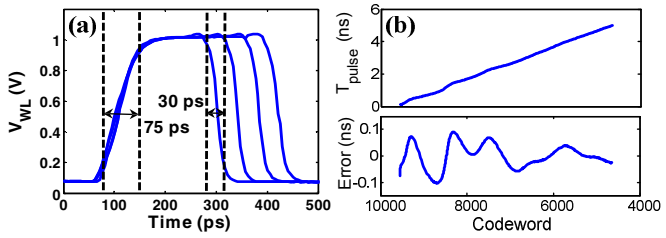


Figure 4 – Plots of (a) multiple subsampled wordline waveforms and (b) codeword to pulse width transfer function.

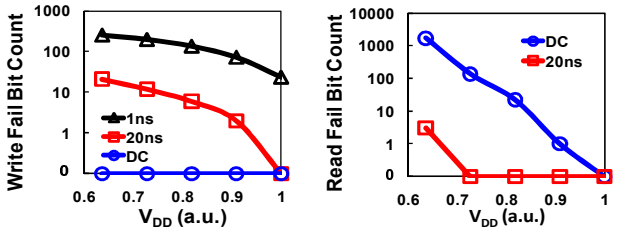


Figure 5 – Fail bit count dependence on V_{DD} and pulse width. Read case only considers read stability and not read access time.

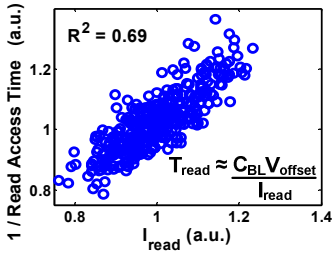


Figure 6 – Scatter plot of read current (I_{read}) and read access time normalized with sense-amp offset.

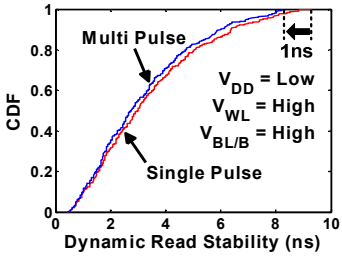


Figure 7 – Statistical distributions of dynamic read stability.

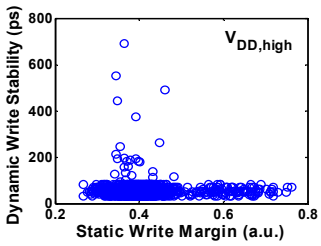


Figure 8 – Dynamic write stability vs. static write margin at $V_{DD,high}$.

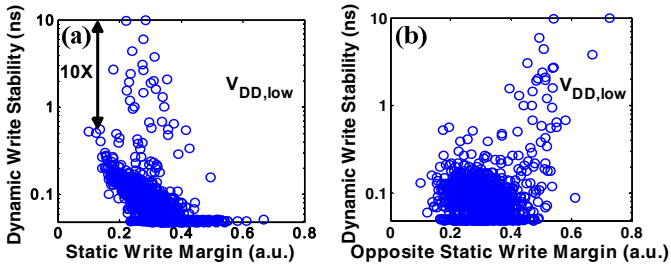


Figure 9 – Dynamic write stability vs. static write margin of (a)similar and (b)opposite side of SRAM cell measured at $V_{DD,low}$.

NBTI Test Procedure:

1. Measure write stability
2. Initialize array to "0" state
3. 2 hour NBTI stress
   V_{DD} = 1.8V
   T = 125°C
4. Measure write stability

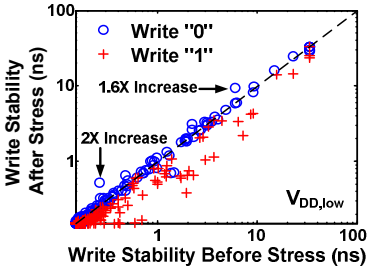
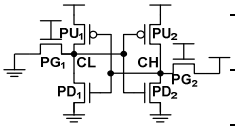


Figure 10 – Write stability degradation due to NBTI.

Table I – Sensitivity analysis of write stability.



	PD1	PG1	PU1	PD2	PG2	PU2
Static (V/V)	0	-0.8	0.6	0.3	-0.3	0
Dynamic (ns/V)	0.02	3.9	-0.7	-0.08	1.0	1.3