A 1–190MSample/s 8–64 Tap Energy-Efficient Reconfigurable FIR Filter for Multi-Mode Wireless Communication

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Abstract

An energy-efficient reconfigurable distributed-arithmetic FIR filter for multi-mode wireless communication is fabricated in 7M1P 90nm CMOS and occupies 1.5mm^2. A 6-way parallel, 2-way time-multiplexed architecture with circuits for memory offset binary coding and memory partitioning enable input wordlength and tap configurability with 1–190MSample/s throughput and 10–130mW total power measured at 1.1V, 25°C.

Introduction

The diversity of services on hand-held devices mandated by multiple wireless networks implementing a plurality of standards can only be leveraged efficiently by components that can be reconfigured to support each radio standard. In the digital RF front-end, signal processing tasks such as decimation, channel selection, equalization, and sample-rate conversion must be supported by flexible digital FIR filters that consume little power while accommodating low to high throughput rates, varying number of taps and different input wordlengths (Fig. 1). Using an architecture-to-circuit top-down and bottom-up power-performance optimization [1], a reconfigurable distributed-arithmetic (DA) finite impulse response (FIR) filter targeted for a single-chain multi-mode radio transceiver is designed and fabricated in 7M1P 90nm GP CMOS technology. The 1–190MSample/s (1.0Mbps–2.3Gbps) 8–64 tap digital FIR can be configured to support: (i) resampling and equalization for ATSC and DVB-T/H signals, (ii) decimation and channel selection for GSM and UMTS transceivers, and (iii) decimation and low-pass filtering for WLAN 802.11a/g receivers.

Reconfigurable DA FIR Filter Circuit Design

The multiplier-less DA filter pre-computes 2^N input-dependent coefficient sums which are stored in a LUT [2,3]. Bit-slices of the N-input words form addresses used to retrieve coefficient sums from the look-up tables (LUTs) (Fig. 2). The sums are shifted and accumulated to form the filter output [3]. In a fully parallel implementation, each LUT needs to be replicated 12 times for 12b maximum input wordlength. Instead, we employ a parallel, time-multiplexed architecture (Fig. 3) so that only 6 LUT replicas are required, thereby reducing area by 50% while still meeting maximum throughput requirements. A second half-rate clock, CLK2, derived from the system clock supports time-multiplexing. The system clock can be varied from 1MHz up to 380MHz.

Maximum coefficient wordlength of 19b is supported using 22b memory wordlength. The maximum 12b input wordlength is supported using a matrix of 12 x 64b shift-register chains that generate 12 64b LUT addresses. The 12 addresses are divided into two parts. The first 6 addresses correspond to the most significant bit slices of the input word and 63 delayed taps of the previous inputs; the second set of 6 addresses corresponds to the least significant bit slices of the 64 signals. The half-rate clock controls which addresses appear at the read address port of the LUT: when CLK2 is '1', the most significant bit slices are selected as read addresses. Address generator shift registers (FIFO) are clock-gated to reduce power when the filter operates below full capacity.

Memory partitioning of partial coefficient sum LUTs reduces memory size from 2^N to $M \cdot 2^{N/M}$ (where N is the number of taps and M is the number of partitions) (Fig. 4) and enables tap programmability from 8 taps to 64 taps in 8-tap groups. Each LUT module is partitioned into 8 register files and stores pre-computed combinations of coefficient sums for 8 coefficients. Power-gating turns on/off LUT partitions to configure filter order and reduce power when the number of taps is less than 64. Clock-gating LUT partitions enable 2–12b (in steps of 2b) input wordlength programmability.

Memory size is further reduced by 50% using offset binary coding (OBC) [3] on LUT content. OBC reduces memory address size by one bit by XOR-ing each address bit with the MSB. The 64b addresses are fed into an OBC address encoder where it is partitioned into 8 clusters of 8b, followed by XOR-ing of the LSBs with the MSB to form 7b partition addresses, resulting in 56b address words (Fig. 5). The address MSB is used to assign the proper sign to the register file output: if the MSB is "1", the output is negated. As a result total LUT size shrinks from 2^{64} words to 1024 words.

The single LUT add block is comprised of a LUT decoder, partition selector, and partition adder (Fig. 3). The decoder assigns proper sign to the retrieved partial coefficient sum using the sign bit. The partition selector zeros-out unused LUT partition outputs to reduce activity factor of the subsequent tree adder. The pipelined partition adder sums the output of the 8 register files within a single LUT to yield the final pre-computed coefficient sum for a single LUT. The final LUT accumulation performs shifting, accumulation of the LUT outputs and the final summation of the time-multiplexed outputs to generate the filter output.

Measurement Results

The reconfigurable multi-mode transceiver DA FIR test-chip, fabricated in a general-purpose 90nm CMOS process, operates at f_{max} of 380MHz and consumes 130mW (measured at 1.1V, 25°C) in 64-tap, 12b input wordlength mode and occupies 1.5mm^2 core area. Fig. 6 shows the impulse response of the DA FIR configured as a 64-tap, 12b GSM raised-cosine FIR and the impulse response of the DA FIR configured as a 32-tap 10b WLAN bandpass FIR. The DA FIR throughput ranges from 1–190MSample/s with power consumption of 9.5mW–130mW for a full-capacity 64-tap DA FIR, input wordlength range of 2b–12b (Fig. 7). Power consumption varies linearly with number of taps for 12b input wordlength, from 10mW to 130mW across a wide range of throughputs (Fig. 8). Worst-case leakage of synthesized GP memories at 1.1V, 25°C is reduced by 90% to 6mW with power-gating. Leakage can be further reduced by mapping the design onto a low-leakage design library at the cost of lower throughput. The wide throughput range of the flexible DA FIR supports not only targeted ATSC and DVB-T/H broadcast, GSM and UMTS 3G, and WLAN 802.11g/n standards, but also those requiring higher throughput rates, up to 190MSample/s, at <2x area- and energy-efficiency cost of respective dedicated filters.

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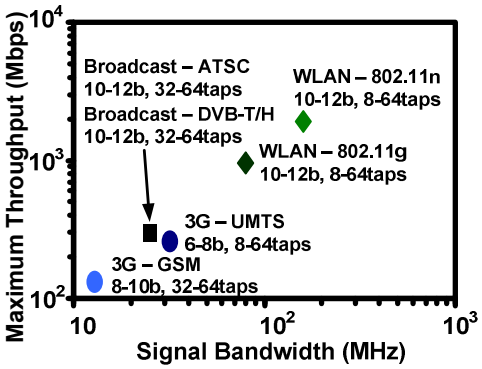


Fig. 1: Flexible FIR specifications

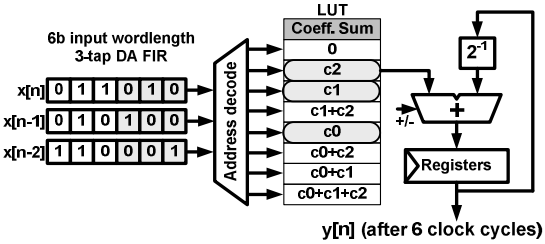


Fig. 2: Simple DA FIR

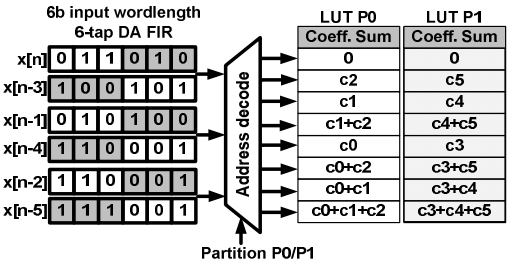


Fig. 3: Memory partitioning

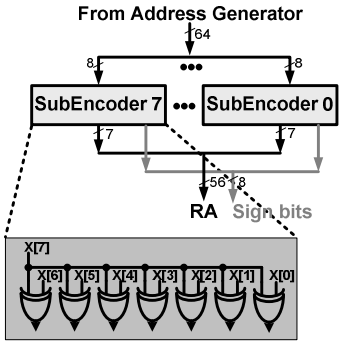
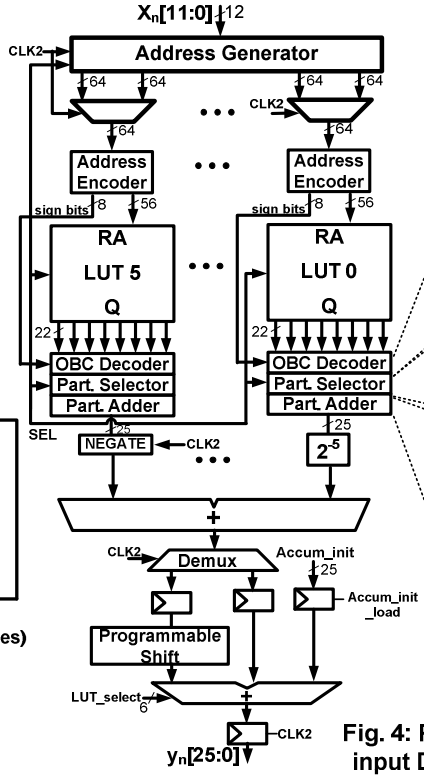


Fig. 5: Address encoder



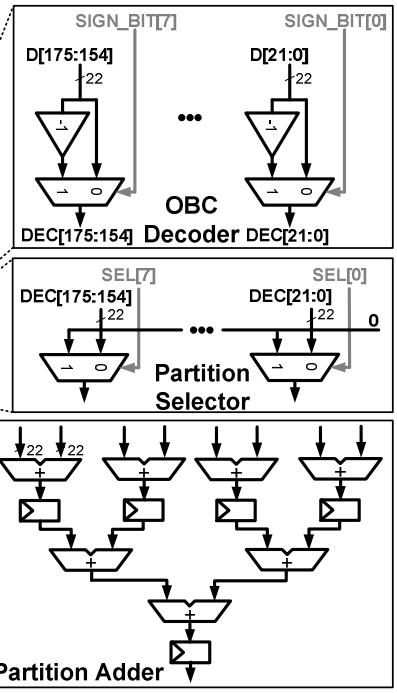


Fig. 4: Parallel, time-multiplexed 8-64 taps, 2b-12b input DA FIR with memory partitioning and OBC

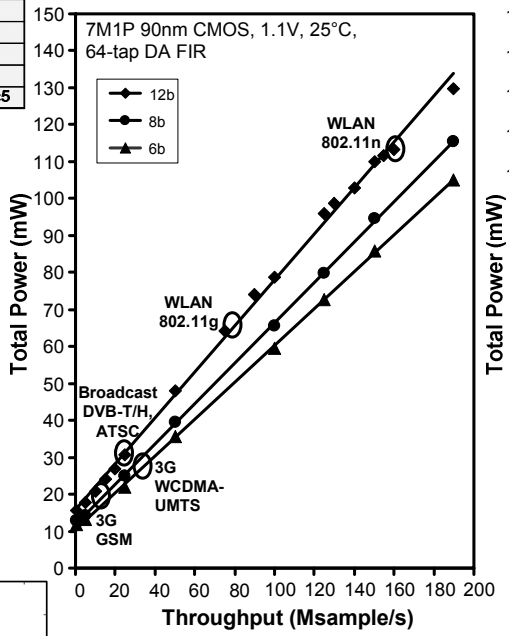


Fig. 7: Input word configurability measurements

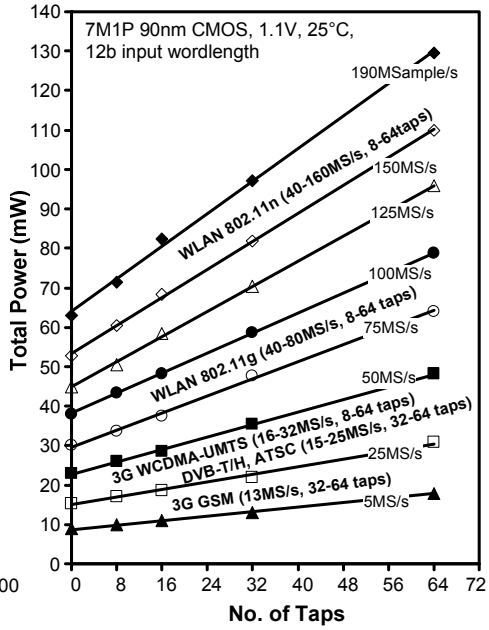


Fig. 8: Tap configurability measurements

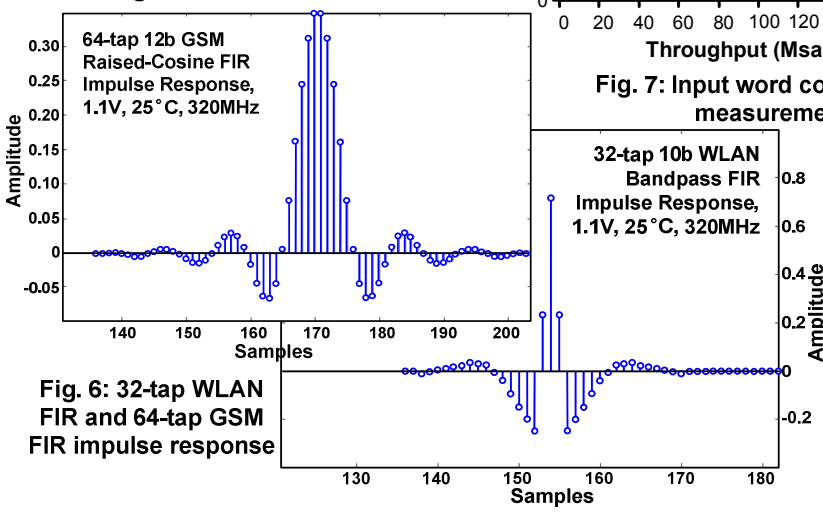
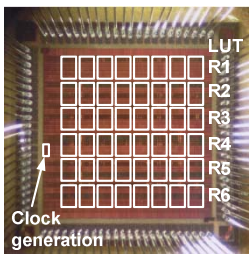


Fig. 6: 32-tap WLAN FIR and 64-tap GSM FIR impulse response



Process	7M1P 90nm CMOS
Core Area	1.5mm²
0-12b, 2b steps 8-64 taps, 8-tap steps	1–190MSample/s (1.0Mbps–2.3Gbps), 10–130mW,1.1V, 25°C
Max. Throughput, 64-taps, 12b input	2.3Gbps, 380MHz, 130mW at 1.1V, 25°C
Worst case leakage power	66mW w/o gating; 6mW w/ power gating, 380MHz, 1.1V, 25°C

Fig. 9: 8-64 tap, 2b-12b input DA FIR performance summary and die photo