Segmented Tri-Gate Bulk CMOS Technology for Device Variability Improvement

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Abstract

Tri-gate bulk MOSFETs are realized using a simple shallow-trench-isolation (STI) oxide recess approach. The tri-gate structure together with a retrograde body doping profile provides for superior electrostatic integrity, particularly for narrow fin widths, to reduce variability in transistor performance. The benefits of tri-gate bulk MOSFET technology for 28nm-node 6-T SRAM cells (0.149um^2 bit-cell area) are assessed. As compared against planar cells, tri-gate cells show less degradation in static noise margin (SNM) and write margin (WRM) variations with decreased operating voltage. Thus, the STI-recess process provides a simple means for reducing device performance variability to facilitate CMOS technology scaling.

Introduction

A challenge for continued CMOS technology scaling, particularly SRAM cell-area scaling, is threshold voltage (V_T) variation due to process-induced variations [1], which ultimately limits voltage scaling [2]. To suppress V_T variation, improved control of short-channel effects (SCE) is required. This can be been achieved by using a retrograde or delta-shaped body doping profile [3] or an advanced transistor structure such as the lightly doped (fully depleted) planar thin-body MOSFET or vertical multi-gate MOSFET [4, 5]. To avoid the need for expensive SOI substrates or very complex fabrication processes, multi-gate MOSFETs can be fabricated on bulk-Si substrates by patterning active regions each consisting of very narrow stripe(s), with width smaller than the minimum gate length, and then selectively etching back the isolation oxide surrounding these narrow active regions to form tall channel fins prior to gate-stack formation [6]. In this work, a timed dilute-HF etch is used to only slightly recess the isolation oxide prior to gate-stack formation, to form tri-gate bulk MOSFETs (with fin widths larger than the gate length) using an otherwise conventional CMOS process flow. The benefits of tri-gate bulk MOSFET technology for 6T-SRAM scaling are demonstrated.

Device Fabrication

Devices were fabricated using a 28nm bulk CMOS process, with the front-end-of-line steps outlined in **Fig. 1**. After the conventional STI process, well formation, and V_T-adjust ion implantation, the STI oxide was slightly recessed by various amounts (all less than the minimum fin width) on selected wafers just prior to gate-stack formation. As a result, tri-gate structures were naturally achieved on these wafers (**Fig. 2**). The experimental splits are described in **Fig. 3**. It should be noted that better electrostatic integrity is expected for tri-gate devices with narrower active ("diffusion") region, *i.e.* smaller physical channel width [7].

Results and Discussion

The electrical channel width is larger for a tri-gate MOSFET than for a planar MOSFET of the same physical width, since the gate electrode wraps the sides of the channel. Together with improved electrostatic integrity, this provides for higher drive current (I_{on}) at a given off-state leakage current (I_{off}), as seen in the scatter plots of **Figs. 4** and **5** for NMOS and PMOS devices, respectively. Thus, the layout efficiency of a tri-gate MOSFET can be improved by increasing the STI oxide recess depth. The recess depth cannot be too large, however; otherwise, SCE will not be adequately suppressed [8].

Improvements in I_{on} variation and 3-sigma/median are also seen for segmented tri-gate (twenty 50nm-wide fins) *vs.* planar (1-um-wide active region) devices, in **Figs. 6** and **7**. Although improved gate control is beneficial for reducing variability in transistor performance, it generally results in reduced V_T due to improved sub-threshold swing (**Figs. 8-11**), which is undesirable because it degrades SRAM static noise margin.

Figs. 12 and 13 show measured I_d-V_g characteristics for segmented tri-gate devices of various fin widths. As expected, drain-induced barrier lowering (DIBL) decreases with decreasing fin width, due to improved gate control of the channel potential. Body biasing can be used to adjust the V_T of a tri-gate bulk MOSFET, as can be seen from the measured I_d-V_d characteristics in **Fig. 14**. This is advantageous for dynamic V_T control to optimize the energy-performance trade-off. The impact of the body-to-source bias (V_{bs}) diminishes with decreasing fin width, however, as the gate control increases.

Fig. 15 compares the degradations in 6-T SRAM SNM and WRM variations (expressed by 3-sigma/median) as the cell operating voltage (V_{dd}) is reduced from 1.0V to 0.8V, for planar (control) *vs.* tri-gate SRAM cells. The increase in variation with V_{dd} scaling is mitigated for the tri-gate technology.

Conclusion

A simple STI-recess step is introduced into a 28nm node CMOS process flow, to achieve tri-gate bulk MOSFETs with improved electrostatic integrity for improved performance and reduced variability. This technology can facilitate SRAM cell-area and voltage scaling in the future.

References

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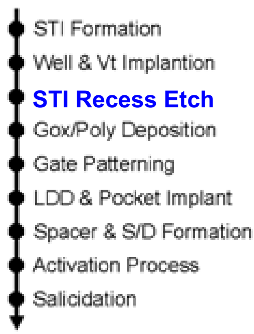


Fig. 1 Key process steps used to fabricate tri-gate bulk MOSFETs in this work.

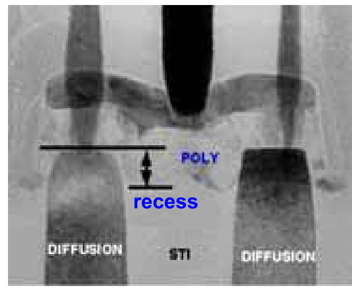
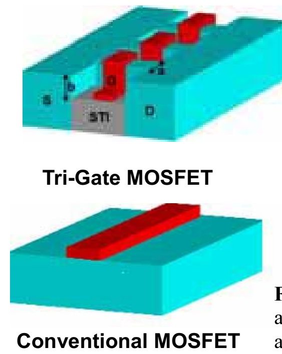


Fig. 2 Cross-sectional TEM image of a tri-gate SRAM cell.



Sample	Recess Condition
Control (Conventional MOSFET)	No recess
Case A	Slightly Recessed
Case B	Recessed
Case C	Very Recessed

Fig. 3 Schematic illustrations of tri-gate and conventional MOSFET structures (left) and experimental splits (right).

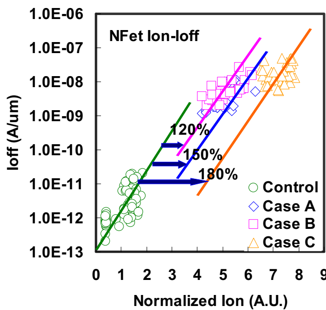


Fig. 4 Comparison of I_{off} *vs.* I_{on} for bulk NFETs of various STI-oxide recess depths. I_{on} is improved by 180% for the very recessed case.

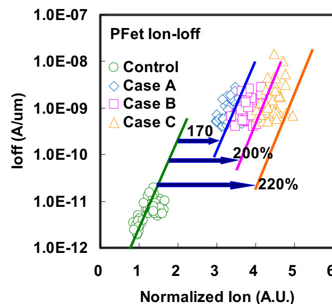


Fig. 5 Comparison of I_{off} *vs.* I_{on} for bulk PFETs of various STI-oxide recess depths. I_{on} is improved by 220% for the very recessed case.

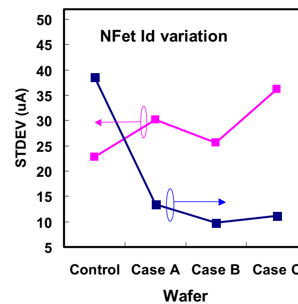


Fig. 6 Comparison of I_{on} variation and 3-sigma/median values for bulk NFETs of various STI-oxide recess depths.

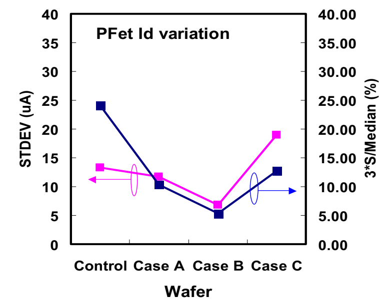


Fig. 7 Comparison of I_{on} variation and 3-sigma/median values for bulk PFETs of various STI-oxide recess depths.

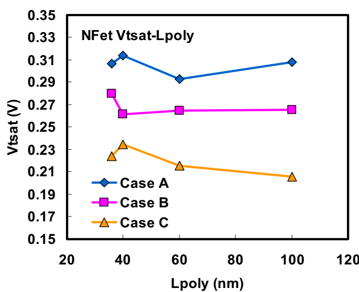


Fig. 8 Comparison of V_T roll-off characteristics for bulk NFETs with various STI-oxide recess depths.

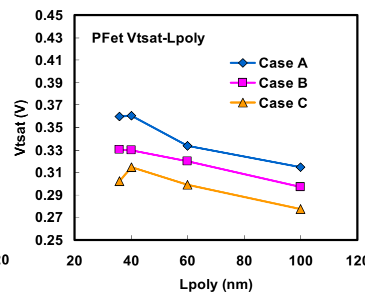


Fig. 9 Comparison of V_T roll-off characteristics for bulk PFETs with various STI-oxide recess depths.

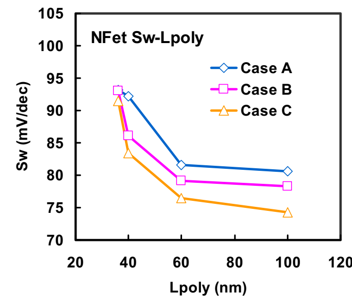


Fig. 10 Measured subthreshold swing *vs.* gate length for bulk NFETs with various STI-oxide recess depths.

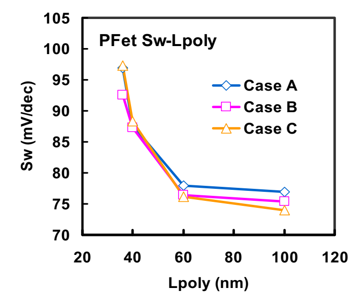


Fig. 11 Measured subthreshold swing *vs.* gate length for bulk PFETs with various STI-oxide recess depths.

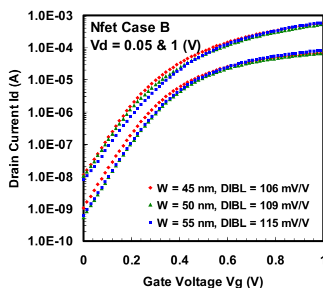


Fig. 12 Measured tri-gate NFET I_d-V_g characteristics, for different fin widths.

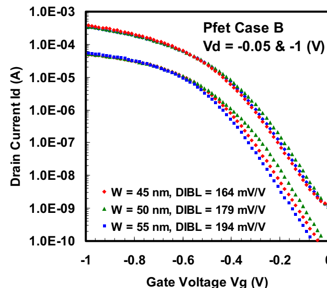
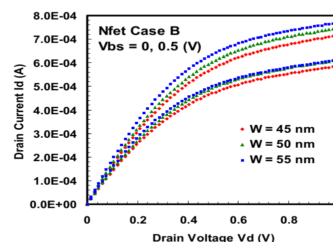


Fig.13 Measured tri-gate PFET I_d-V_g characteristics, for different fin widths.



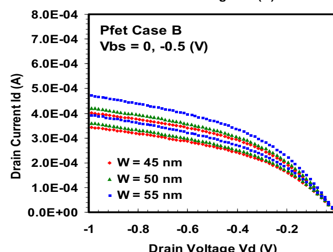
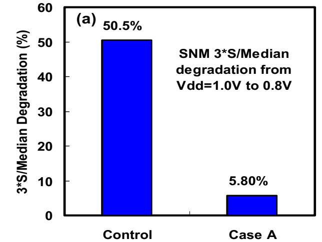


Fig. 14 Measured tri-gate NFET (top) and PFET (bottom) I_d-V_d characteristics, for different fin widths and substrate voltages.



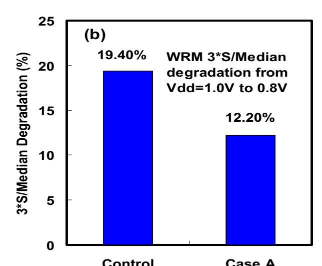


Fig. 15 Comparison of 3-sigma/median degradations in (a) SNM (b) WRM as V_{dd} is reduced from 1.0V to 0.8V.

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