19.7 SRAM Stability Characterization Using Tunable Ring Oscillators in 45nm CMOS

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SRAM yield is often characterized through distributions of static read or write margins [1] [2]. These measurements are analog and therefore can be slow and provide a limited dataset. Distributions of per-cell minimum operating voltages can be characterized rapidly, however, and are often taken as a proxy to static noise margins. Both methods have a common limitation in that the characterization is done statically, thus ignoring any possible effects that may affect dynamic operation. Pulsed ring oscillators for evaluating SRAM cell read timing have been previously proposed [3]. In contrast, tunable ring oscillators (RO) for characterizing dynamic cell stability during write and read operations without the need to modify the SRAM array are demonstrated in this work. The performance variation is captured as a spread in RO operating frequencies and therefore can be obtained rapidly.

Figure 19.7.1 shows a schematic view of the write RO wherein a single end of the selected cell is connected to the write RO circuit. The BL switches are implemented using thick gate oxide, long channel, wide transmission gates modulated by separate, elevated power supplies to suppress noise currents and to enable accurate fluctuational characterization down to low operating voltages [1].

The write RO consists of three segments: an enabling stage, intermediate signal restoration stages, and a final weak pull-up stage. The enabling stage initiates the oscillating behavior when the enable signal is asserted. The intermediate stages restore the digital waveforms, which are then fed to a frequency divider coupled to the external pads. The final driving stage is a differential inverter with current-starved pull-up. While the strong pull-down guarantees a new value written into a cell every cycle, the weak pull-up slowly charges up the BL before triggering the next oscillation cycle. The write RO is designed to oscillate in a fashion that emulates continuous write cycles to alternating halves of the cell, with the goal of correlating the oscillation frequency to a write metric of interest. The RO provides analog tuning through *Vctr* to adjust the strength of the weak pull-up.

The write RO frequency is strongly dependent on the combined pull-up strength of the cell and the current-starved RO, and Fig. 19.7.2a shows the relevant current contributions. The RO current dominates if *Vctr* is low. It is desirable to operate the write RO with the cell current dominating to achieve good sensitivity to the current from an individual cell. As shown in Fig. 19.7.2b, the frequency of the write RO correlates well (R^2 of 0.92) with the write trip current (WTI) metric. Although WTI is a static current metric [4], it reflects dynamic behavior of SRAM cells more effectively than static voltage metrics during the write operation. Measuring WTI, however, requires access to internal nodes, which is impractical in dense SRAM arrays.

Figure 19.7.3 shows a schematic view of the read RO wherein a selected cell is differentially connected to the read RO circuit. The read RO consists of three segments: a sensing stage, intermediate restoration stages, and a final driving stage. The sensing stage is a PMOS-skewed inverter with high switching threshold to match typical BL differentials (few 100s of mV from V_{DD}). In order to have the RO oscillation frequency strongly depend only on the BL discharging by the cell, the output of the initial sensing stage is fed to an inverted WL decoder to turn off the WL during the precharge phase of the oscillation. The intermediate stages restore the digital waveforms, which are then fed to a frequency divider coupled to the external pads. The final driving stage consists of a PMOS-skewed inverter with current-starved pull-down. The strong pull-up quickly precharges the BL while the WL is deactivated, and the weak pull-down discharges the BL. The RO provides analog tuning through *Vctr* to adjust the nominal oscillation frequency such that the RO pull-down current is small or comparable to that of a cell read current.

It is desirable to observe the cell read current at lower cell supplies. Lowering the array supply voltage V_{CELL} can magnify the effect of read disturbance that raises the internal node voltage that stores a "0." Doing so effectively weakens the corresponding pull-down transistor, allowing the internal node to rise up to a higher voltage.

Figure 19.7.4a illustrates the variation in read current as V_{CELL} is swept. A higher read current at nominal voltages does not necessarily translate to a higher read current at lower V_{CELL}. Right before the cell fails data retention, denoted by the sharp drop in I_{READ} (at $V_{CELL,CRIT}$), the corresponding pull-down transistor is at its weakest. Therefore, if a half cell can still exhibit high read current at that point, it must have a relatively strong pull-down and therefore good dynamic recoverability. It would be desirable to operate the read RO at a $V_{CELL,OPT}$ that is slightly greater than the rightmost $V_{CELL,CRIT}$.

Figure 19.7.4b shows a good correlation (R^2 of 0.84) between the frequency of the read RO and the static current noise margin (SINM) at optimal V_{CELL}. The correlation is stronger for cells closer to failure. SINM is a static current metric [5] which reflects the dynamic behavior of SRAM cells more effectively than static voltage metrics during the read operation. Measurement of SINM, however, also requires access to internal storage nodes, which is impractical in dense SRAM arrays.

Figure 19.7.5 depicts the photo of the die fabricated in a 45nm CMOS process. There are four separate SRAM arrays: 2 arrays are 128*256 and 2 arrays are 64*256. The SRAM cell size is 0.252 um^2. The entire RO block measures 190um by 66um, which presents a very small area overhead to the overall SRAM array. Primary overhead is in the BL switch matrix that is shared between the RO and the static noise margin measurement circuits.

Figure 19.6.6 shows the measured correlation between the write RO frequency and the WL write trip voltage (WWTV) defined in [2], which is a static write metric measured in a large array without accessing internal nodes. The write RO is tuned to have the cell pull-up drive strength dominate the RO pull-up drive strength. The measurements are taken at a V_{CELL} of 1.1 V, 0.9 V, and 0.7 V show an R^2 of 0.55, 0.65, and 0.63 respectively. The relatively low R^2 is due to the fact that WWTV (a voltage metric) does not correlate strongly with WTI (a current metric).

Figure 19.7.7a shows the measured correlation between read RO sensitivity and the cell read current. To account for intrinsic bit-line loading in different columns, read RO sensitivity is defined as the difference between the oscillation frequencies of the RO when WL is asserted and de-asserted divided by the frequency when WL is asserted. The read RO sensitivity correlates strongly with cell read current with R^2 of 0.84, 0.94, and 0.98 at V_{CELL} of 1.1 V, 0.9 V, and 0.7 V respectively. Correlation between read RO sensitivity and read current increases at lower V_{CELL}. Moreover, Fig. 19.7.7b shows that read current correlates with SINM with R^2 of 0.60 when the read current is measured at $V_{CELL,OPT}$. Because read RO sensitivity correlates well with read current, the read RO can be used to measure SINM without accessing internal storage nodes.

Acknowledgments:
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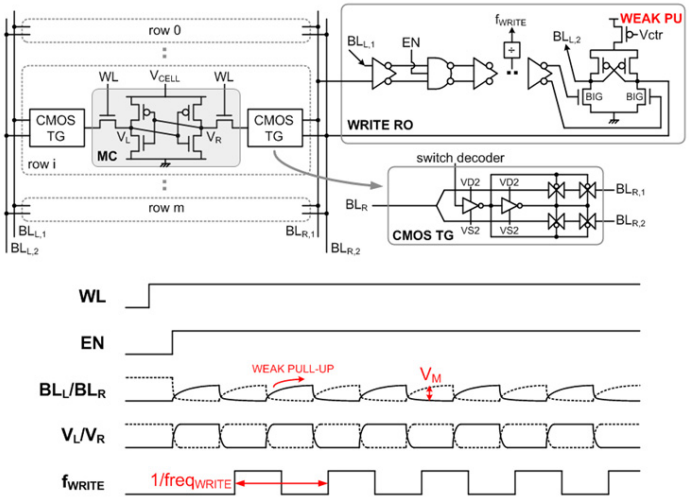

Figure 19.7.1: Write ring oscillator schematic showing a weak differential pull-up driver that writes a new value into an SRAM cell once every oscillation cycle

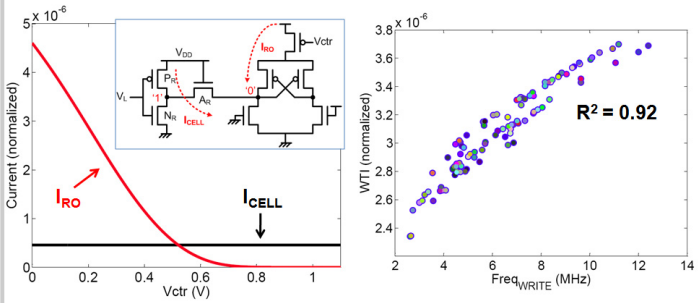

Figure 19.7.2: Correlation of WTI and $Freq_{WRITE}$ (a) Pull-up current contribution versus Vctr (b) Simulation of WTI versus $Freq_{WRITE}$ at Vctr = 1.1 V

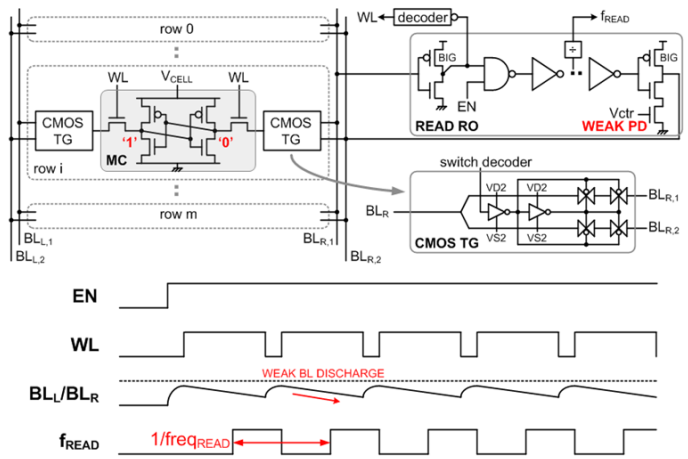

Figure 19.7.3: Read ring oscillator schematic showing a weak pull-down driver that strongly charges the BL and then weakly discharges the BL every oscillation cycle

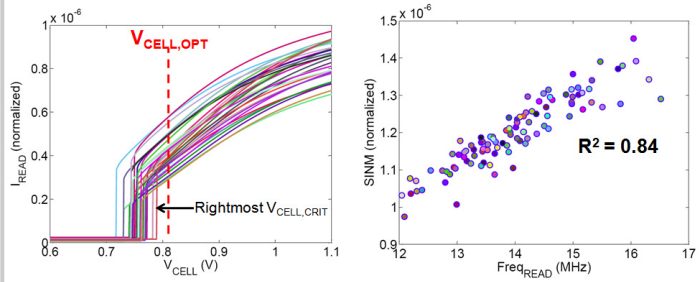

Figure 19.7.4: Correlating SINM and $Freq_{READ}$ by magnifying read disturbance (a) Simulation of I_{READ} as V_{CELL} is lowered (b) Simulation of SINM versus $Freq_{READ}$ at $V_{CELL,OPT}$

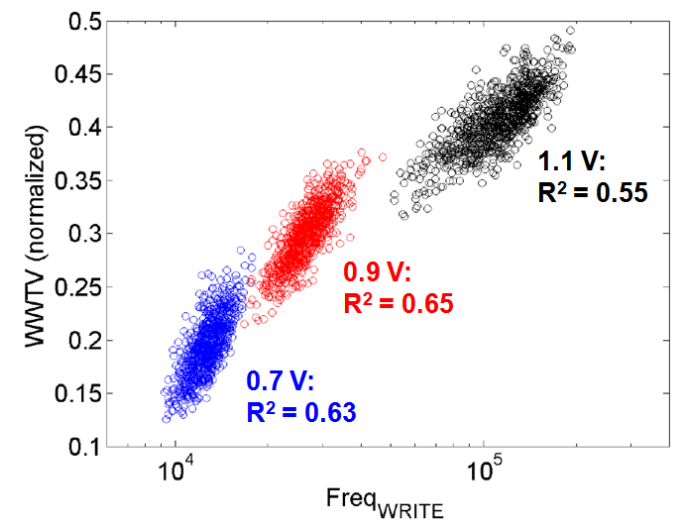

Figure 19.7.5: Measured Write RO Frequency (LOG) vs. WWTV as V_{CELL} is lowered

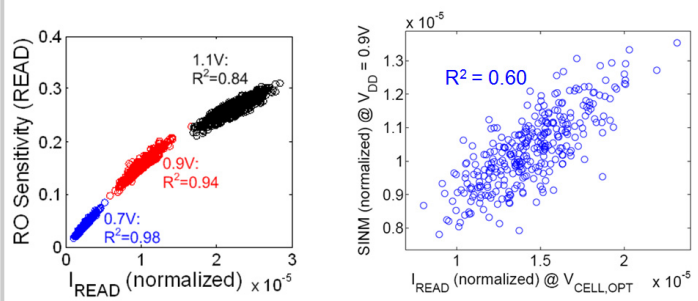

Figure 19.7.6: Correlating SINM and Read RO Sensitivity (a) Measured Read RO Sensitivity vs. I_{READ} (b) Measured SINM versus I_{READ} at $V_{CELL,OPT}$

19

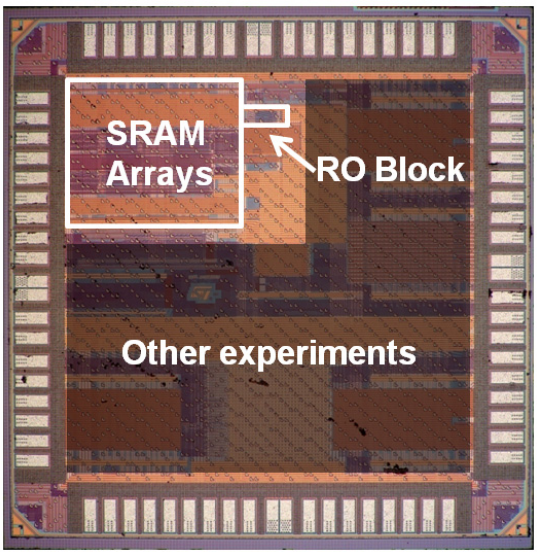

Figure 19.7.7: Die fabricated in 45nm CMOS.

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