SRAM Design in Fully-Depleted SOI Technology

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***Abstract*— Continued increase in variability is a challenge for SRAM scaling into sub-22nm nodes, and presents an opportunity for the introduction of alternate technologies. In this work, the performance and threshold-voltage variability of vertical SOI finFETs are compared against those of planar fully depleted (FD) SOI MOSFETs with thin buried oxide, and are presented as an alternative to planar bulk CMOS. Analytical modeling derived from 3D device simulations is used to estimate six-transistor SRAM cell performance and yield metrics.**

I. INTRODUCTION

Technology scaling reduces minimum features by a factor of 0.7 in every new technology generation, which enables scaling of the conventional six-transistor (6T) SRAM cell area by a half. Increasing variation in transistor parameters with continued scaling is a major challenge for continued bulk/PD-SOI CMOS technology advancement [1,2]. In particular, relative effects of random variations in threshold voltage (V_{TH}) due to random dopant fluctuations (RDF) and gate line-edge roughness (LER) will increase significantly as the gate length (L_G) is scaled down below 30 nm [3]. Increased transistor mismatch results in a higher variation in SRAM cell design margins [4]. Simultaneously, smaller cell sizes enable larger cache memory arrays, requiring designs to satisfy wider design margins to ensure appropriate yield. The requirements to satisfy cell stability margins 6 or 7 standard deviations away from the mean threaten to limit cell-area scaling and/or operating voltage (V_{DD}) reduction. In the present bulk/PD-SOI CMOS technology designs, required array yield is guaranteed through either larger SRAM cell sizes, increased transistor counts in the cell [6], or additional peripheral circuitry that enhances the read stability or writeability of the cell [6]. Each of these techniques increases the effective cell area, which is the overall area of the array including the peripheral circuitry, divided by the number of cells. This potentially reduces the benefits of technology scaling and presents an opportunity for an alternate technology that can enable smaller SRAM cells, and lower overall design cost. Advanced transistor structures which suppress short-channel effects more effectively than conventional bulk/PD-SOI MOSFET structures, without the need for heavy channel doping, are being explored for sub-22 nm CMOS technology nodes.

The finFET [4] offers the improved electrostatic integrity of a double-gate MOSFET structure and has a process flow and layout similar to that of the conventional MOSFET [8]. In order to effectively suppress short-channel effects (SCE), the thickness of the body (*i.e.* the fin width) should be no greater than 2/3 times the gate length (L_G) [8]. In order to minimize RDF effects, the body should be undoped [9]. Fin LER is a potential issue, but can be mitigated by using spacer lithography [10]. 6-T SRAM cells fabricated with finFETs have been reported to achieve improved performance for comparable write and static noise margins, as compared with cells fabricated with planar MOSFETs [9].

The FD-SOI MOSFET structure with a very thin (~10 nm-thick) buried oxide (BOX) layer and a heavily doped substrate ("ground plane") has been shown to be effective for reducing the impact of parameter variations and RDF, due to its excellent electrostatic integrity and the elimination of body doping [11]. FD-SOI layout is nearly identical to bulk, and design migration is straightforward. Recently, functional SRAM cells were demonstrated using such FD-SOI devices, for the 32 nm technology node and beyond [12].

The key enabler for FD-SOI designs is the availability of SOI wafers with very uniform Si thicknesses, with variation less than 0.5nm [13]. The threshold of the FDSOI device is strongly dependent on the body thickness, and the variation control better than 0.5nm enables scaling of gate lengths to well beyond 22nm.

This paper reviews recent results for SOI finFET and thin-BOX FD-SOI technologies [14, 15], and via 3D atomistic process and device simulations compares them with the bulk MOSFET technology at the 22 nm technology node, with analytical modeling for SRAM yield estimation. In addition, iso-area and iso-yield comparison between the FD-SOI and the bulk cells are shown.

II. MOSFET DESIGNS

Fig. 1.a and 1.b. shows illustrations of the finFET and FD-SOI MOSFET designs analyzed in this work. In both designs, the gate length (L_G) is 25 nm, the equivalent gate-oxide thickness (T_{ox}) is 1 nm, and the body is undoped.

FinFET design parameters are summarized in the table in Fig. 1.a**.** The fin width (W_{fin}) is 2/3 times L_G in order to suppress SCE, and the fin height (H_{fin}) is 4/3 times L_G in order to achieve layout efficiency comparable to planar MOSFET technology. For compact circuit layouts such as those used in SRAM cells, it is difficult to separately engineer the gate work functions (Φ_M) of the pull-down (PD) and pull-up (PU) devices because the gate layer fills the entire region in-between the n-channel and p-channel fins [15]. Therefore, a single near-midgap gate work function is assumed. The

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electrical channel length (L_{eff}) was selected to maximize drive current (I_{ON}) for an off-state leakage current (I_{OFF}) of 3 nA/µm (ITRS specification for low-operating-power (LOP) applications [16]). Table 1 provides a summary of device performance parameters. It should be noted that the electrical channel width of a finFET is $2H_{fin}$ [18]. In practice, effective width can only be changed in increments of $2H_{fin}$, by using multiple fins in parallel, which requires discrete adjustments in the β ratio of a finFET SRAM cell and can present a significant cell-area trade-off.

Thin-BOX FD-SOI device design parameters are summarized in the corresponding table in Fig. 1.b., and were selected to mimic the design from [19] for superior short-channel effect control and to allow for effective back-bias. The structure in [19] is fabricated using an implantation-free process to avoid dopant straggling and damage-induced defects in the thin body region [19], to reduce RDF-induced variations. The process uses a low temperature, zero-silicon-loss epitaxial growth process to form (faceted) *in-situ*-doped (10^{20} cm^{-3}) raised-source/drain regions – from which dopants are diffused to form the lightly doped source/drain extensions to reduce series resistance with minimal increase in sidewall gate capacitance [19]. Φ_M values were selected to achieve the LOP ITRS specification for off-state leakage current (I_{OFF}), ~3nA/µm. For comparison, a planar bulk MOSFET design (Fig. 1.c.) with uniform channel doping profile (10^{18} cm^{-3} B), doped poly-Si gates, and comparable I_{OFF} were also simulated, using the design parameters in **Fig. 1.c**.

A simple analytical model [20] was fit to the simulated current-voltage characteristics for each MOSFET design, to allow for fast estimation of SRAM metrics such as read static noise margin (RSNM) [21] and writeability current (I_w) [22]. Variation in saturation threshold voltage ($V_{T,SAT}$) due to RDF was evaluated using 3D Kinetic Monte Carlo simulations (100 cases for each nominal design). $V_{T,SAT}$ variation due to gate LER was evaluated using 100 different gate-line profiles derived from a scanning electron microscopy image of photoresist lines processed for the 22 nm node. $\sigma(V_{T,SAT})$ due to gate work function variation (WFV) is estimated based on [23]. These random sources of variation are assumed to be statistically independent, and their additive impacts on $\sigma(V_{T,SAT})$ for finFET and FD-SOI SRAM pull-down devices are indicated in Tables 1 and 2, respectively, along with other nominal electrical parameters. The FD-SOI structure has smaller $\sigma(V_{T,SAT})$ due to its superior electrostatic integrity.

III. 6-T SRAM CELL DESIGNS

The cell layout parameters are summarized in Figure 2. These values are obtained by linearly scaling the finFET-based SRAM cell in [24] and by following the 22 nm design rules in [25].

Table 1: FinFET electrical parameters.

	n-type	p-type
I_{ON} (µA/µm)	918	563
I_{OFF} (nA/µm)	3	3
$\|V_{T,LIN}\|$ (mV)	200	241
$\|V_{T,SAT}\|$ (mV)	123	135
DIBL (mV/V)	86	118
S.S. (mV/dec)	78	84
$\sigma V_{T,SAT}$ (mV)$\|_{LER}$	29	39
$\sigma V_{T,SAT}$ (mV)$\|_{LER+RDF}$	31.3	43.7
$\sigma V_{T,SAT}$ (mV)$\|_{LER+RDF+WFV}$	32.9	44.9

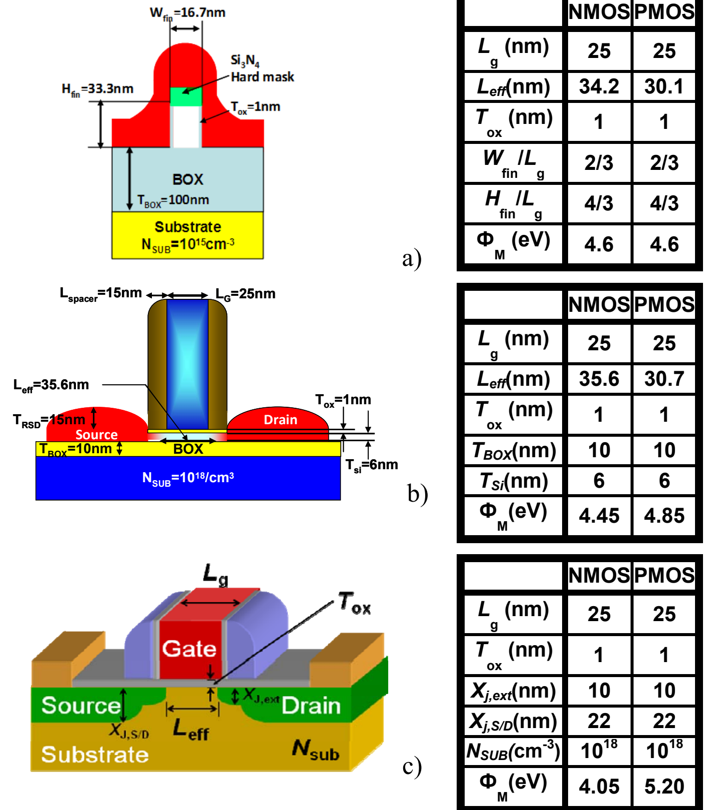

Figure 1: Illustrations of the device structures studied in this work: a) SOI finFET cross-section, b) FD-SOI MOSFET cross-section, c) bulk MOSFET cross-section. Device parameters are indicated in tables next to each design. Ohmic contacts are made to the top surfaces of the source and drain regions.

For a finFET-based SRAM cell, such as one in Fig. 3, the cell β ratio is either 1 if single-fin-PD devices are used or 2 if dual-fin-PD devices are used. As a result, there is a significant increase in cell area (0.075 µm^2 *vs.* 0.085 µm^2 for single-fin-PD *vs.* dual-fin-PD cells) for improved read margin (142 mV *vs.* 190 mV for single-fin-PD *vs.* dual-fin-PD cells, at V_{DD} = 0.9V), unless a pitch-halving technique such as spacer lithography [19] is used to pattern the fins. The FD-SOI cell (with β ratio = 1.375) is as compact as the single-fin-PD finFET cell and offers a read margin (186 mV) that is comparable to that of the dual-fin-PD finFET cell, Fig. 4. The bulk cell has an SNM of 207mV as a result of its higher threshold voltage. Due to higher I_{ON}, I_w is significantly higher for the finFET cells (33 µA and 28 µA for single-fin-PD and dual-fin-PD cells, respectively, at V_{DD} = 0.9V) than for the FD-SOI cell (19 µA), and for the bulk cell (11µA), Fig. 5.

Table 2: FDSOI MOSFET electrical parameters.

	n-type	p-type
I_{ON} (µA/µm)	861	518
I_{OFF} (nA/µm)	3	3
$\|V_{T,LIN}\|$ (mV)	160	182
$\|V_{T,SAT}\|$ (mV)	114	116
DIBL (mV/V)	51	73
S.S. (mV/dec)	75	78
$\sigma V_{T,SAT}$ (mV)$\|_{LER}$	10	14
$\sigma V_{T,SAT}$ (mV)$\|_{LER+RDF}$	22.3	26.1
$\sigma V_{T,SAT}$ (mV)$\|_{LER+RDF+WFV}$	25.5	28.9

Table 3: Summary of the design rules.

Design rules		Symbol	Size [nm]
Cell Height	PG CH length	L_{PG}	25
	PD CH length	L_{PD}	25
	CONT size	X	30
	Gate-to-CONT	Y	20
	Total	190	
Cell Width	POLY-to-POLY	A	30
	POLY-to-DIF ext	B	20
	PD Width	W_{PD}	55
	N/P isolation	C	50
	PU width	W_{PU}	32
	DIF-DIF (min)	D	50
	PG width	W_{PG}	40
	Total	394	
A SRAM cell area		$0.07486\ \mu m^2$	

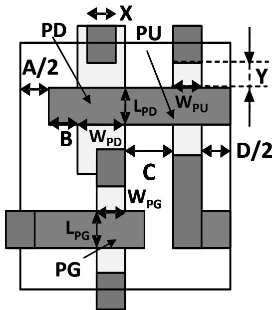

Figure 2: Illustration of the SRAM cell layout parameters.

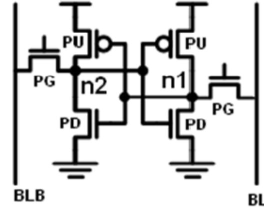

Figure 3: Schematic of the 6T SRAM cell.

IV. Estimated SRAM Cell Yield

Cell sigma, defined as the minimum amount of variation needed to cause a read or write failure [27], is used to assess SRAM yield. Random variations due to gate-LER, RDF and WFV, as well as process-induced variations (±10% at 3σ) in L_G, T_{ox}, Si fin/channel width, and Si height/thickness are considered herein. Figs. 6 and 7 show that the bulk and the single-fin-PD finFET SRAM cell cannot meet the six-sigma yield requirement for read nor write. With increased Φ_M, the dual-fin-PD finFET SRAM cell may meet this requirement, although the minimum cell operating voltage (V_{min}) likely would be higher than that of the FD-SOI SRAM cell. This is due to the larger sensitivities of the finFET to random and process-induced variations, and is consistent with the findings in [9] and [24].

V. Iso-Area and Iso-Yield Comparison

In the previous section, the FD-SOI cell can satisfy the six-sigma yield requirement in reading and writing operations, as compared to the bulk cell. Fig. 8 shows how much yield enhancement in the FD-SOI cell can be achieved quantitatively: The FD-SOI cell with W_{PG}=40nm can maximize read(write) cell sigma, as compared to the optimal bulk cell design with W_{PG}=35nm. On the other hand, the bulk cell needs to be enlarged to satisfy >6σ yield, a pull-down and pull-up transistor widths should be widened to W_{PD}=95nm and W_{PU}=50nm, respectively, for the bulk cell in order to meet the six-sigma yield requirement for read and write operations, resulting in the 40% enlarged bulk cell area (from ~0.07μm^2 to ~0.1μm^2). The spot-lighted design point corresponds to W_{PG}=65nm in the enlarged bulk cell.

VI. Conclusions

Although large cache arrays have been demonstrated to be functional in a high-performance 22nm bulk CMOS technology, there remains an opportunity for alternate technologies to enter the massive low power market because of SRAM scaling challenges. Both planar thin-BOX FD-SOI and finFET designs demonstrate lower variability, which can be used for designing smaller cells than in the bulk CMOS. FinFET SRAM cannot easily meet the six-sigma yield requirement for both read and write operations, if a single-gate-workfunction is used.

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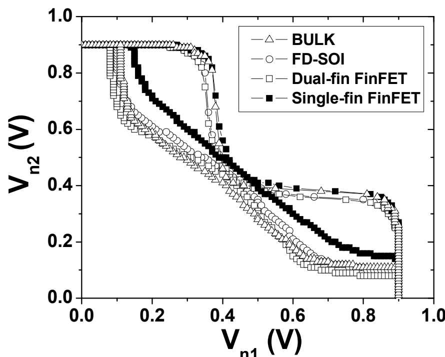

Figure 4: Read SNM simulations for bulk, 1- and 2-fin-PD finFET and FD-SOI SRAM cells.

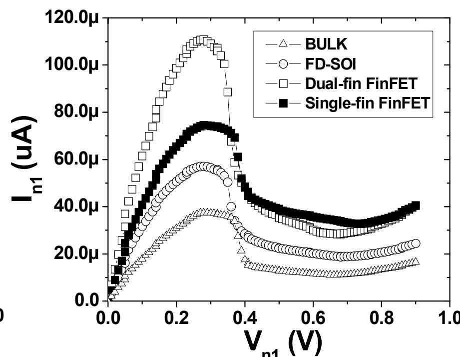

Figure 5: Simulation of the writeability curves for the bulk, 1- and 2-fin-PD finFET and FD-SOI SRAM cells.

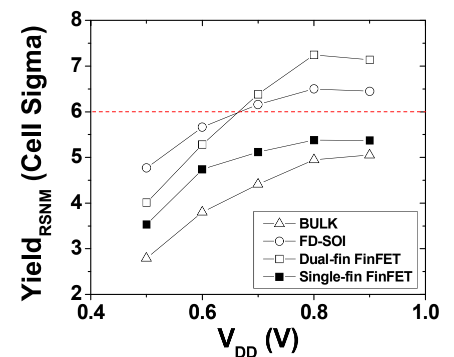

Figure 6: Predicted yield of analyzed SRAM cells during read operation.

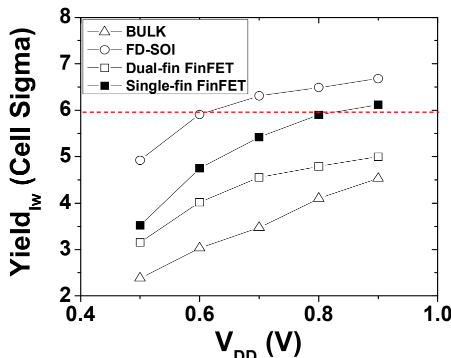

Figure 7: Predicted yield of analyzed SRAM cells during write operation.

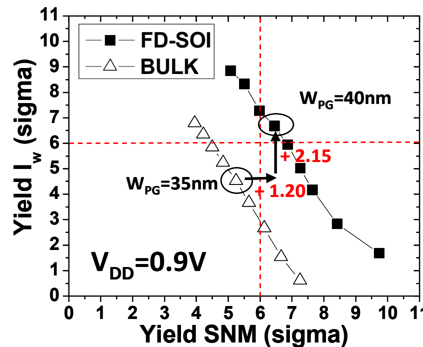

Figure 8: Yield of SNM *vs.* Yield of I_w. (The value of W_{PG} is varied along each curve.) The yield-aware optimal design points for bulk and FD-SOI cells are spot-lighted.

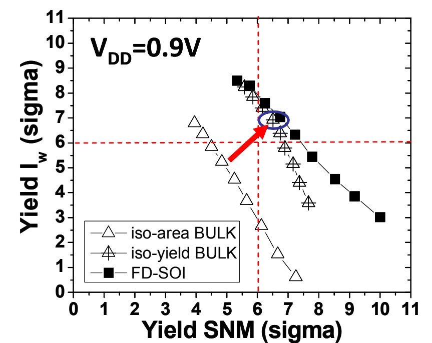

Figure 9: Yield of SNM *vs.* yield of I_w: A larger bulk cell can achieve comparable yield of the FD-SOI cell.