Analysis of the Relationship between Random Telegraph Signal and Negative Bias Temperature Instability

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***Abstract*— Random telegraph signal (RTS) is shown to be an intrinsic component of the shift in MOSFET threshold voltage (V_{th}) due to bias temperature instability (BTI). This is done by starting from a well-known model for negative BTI (NBTI), to derive the formula for RTS-induced V_{th} shift. Based on this analysis, RTS simply contributes an offset in NBTI degradation, with an acceleration factor that is dependent on the gate voltage and temperature. This is verified by 3-dimensional (3-D) device simulations and measurements of 45nm-node bulk-Si PMOS transistors. It has an important implication for design of robust SRAM arrays in the future: design margin for RTS should not be simply added, because it is already partially accounted for within the design margin for NBTI degradation.**

Keywords-component; random telegraph signal; negative bias temperature instability; hole traps; SRAM

I. INTRODUCTION

Random telegraph signal (RTS) is a temporal variation in $I_{ds}(V_{th})$ caused by the capture and emission of mobile charge carriers, and it has been studied for over two decades [1-6]. Since the amplitude of RTS is proportional to the inverse of the MOSFET channel area [3], memory devices manufactured using the most advanced fabrication technologies are facing severe challenges due to this phenomenon. Being different from flash memory devices which have thick gate-oxide films, SRAM devices until recently were not considered to be seriously affected by RTS because they utilize thin gate-oxide films in accordance with MOS scaling [7]. However, because V_{th} variation due to RTS eventually (with scaling) will become comparable to that due to random dopant fluctuations (RDF) [5] – a major source of degradation in SRAM characteristics [8] –studies of the impact of RTS on highly scaled SRAM have been reported [9-12]. Although it is still controversial how much the SRAM minimum operation voltage (V_{min}) is degraded by RTS, SRAM designers should allocate some design margin for RTS in addition to a (larger) design margin for RDF. Furthermore, degradation in PMOS V_{th}, *i.e.* negative bias temperature instability (NBTI) [13-15], should be considered. With the advent of high-k/metal-gate transistors in SRAM, V_{min} degradation due to positive bias temperature instability (PBTI) will also be significant [16, 17].

There is therefore a need to establish appropriate design margins to guarantee sufficient SRAM yield for operation at V_{min}, at minimum cost (*i.e.* without overdesigning the cells). In this regard, it is necessary to account for inter-dependencies between the physical phenomena that cause V_{th} variation and degradation. Islam *et al.* introduced a model for NBTI comprising two components, associated with hole traps and with interface traps [18, 19]. The effect of hole trapping appears for short stress times and eventually saturates at some constant value. On the other hand, interface trapping (attributed to dangling Si-H bonds at the Si-SiO_2 boundary) follows a power-law relationship with stress time and is the dominant component of V_{th} degradation for long stress times. This behavior has been observed experimentally [20], so it is recognized to be a plausible explanation of the NBTI effect. Meanwhile, RTS has been explained to be due to hole trapping/detrapping, and therefore should be related to NBTI. In fact, Kaczer *et al*. pointed out a broad similarity between the relaxation process of NBTI and 1/f noise [21]. Furthermore, Grasser *et al.* succeeded in reproducing the time constants of RTS by using a recovery model of NBTI [22], which indicates that care must be taken to properly account for these two phenomena for worst-case SRAM design margins.

In this paper, a relationship between the V_{th} degradation of RTS and that of NBTI is established, to allow for minimization of design margin. This paper is organized as follows. In section II, the relationship between RTS- and NBTI-induced V_{th} degradation is derived from theory. In section III, the theory is verified by analyzing device simulation results and some measured data for SRAM fabricated using 45nm CMOS technology. Finally, in Section IV, conclusions are drawn.

II. THEORETICAL ANALYSIS

V_{th} degradation due to NBTI is modeled as the sum of an interface-trap effect (ΔV_{IT}) and a hole-trap effect (ΔV_{H}) [18]:

$$\Delta V_{th} = \Delta V_{IT} + \Delta V_{H} = a\frac{q\Delta N_{IT}(t)}{C_{ox}} + \frac{\int_0^{Tox}\int_E x\rho_H(x,E,t)dEdx}{C_{ox}T_{ox}} \quad (1)$$

where a is the fraction of donor-like traps, ΔN_{IT} is the areal density of interface traps, C_{ox} is the areal gate capacitance, T_{ox} is the gate oxide thickness, and ρ_H is the areal charge density due to trapped holes in the gate oxide, respectively. The first term is dominant at long stress times, and shows a power-law relationship with stress time t; it is proportional to t^n, where n ranges from 1/6 to 1/3. The second term saturates at some

value within a relatively short time (milliseconds). According to [18],

$$\rho_H(x,E_i,t) = N_0\delta(E-E_i)f_T(x,E_i,t) \qquad (2)$$

where N_0 is the areal density of pre-existing traps within the gate oxide and E_i is the energy level of the trap. f_T is the probability that a hole trap is filled, which evolves with time:

$$\frac{df_T}{dt} = \sigma \cdot v_{th} \cdot \left[p_h T_1(1-f_T) - n_S T_1 f_T - n_G T_2 f_T\right] \qquad (3)$$

where σ is the capture cross-section, v_{th} is the thermal velocity, p_h is the inversion-layer hole areal density, and n_S and n_G are the areal concentrations of states in the substrate and in the gate, respectively. T_1 and T_2 are the probabilities for tunneling between the substrate and the gate oxide, and for tunneling between the gate oxide and the gate, respectively. This equation was solved in [18] for the initial condition $f_T(0) = 0$, *i.e.* zero initially trapped holes. Taking RTS into consideration, however, $f_T(0)$ should have a non-zero value. We therefore propose to separate f_T into a shallow-trap term $f_{T\text{-}S}$ and a deep-trap term $f_{T\text{-}D}$, and subsequently focus on $f_{T\text{-}S}$ since the derivation of $f_{T\text{-}D}$ is the same as that given in [18]. From [23], $f_T = \tau_e/(\tau_e+\tau_c)$ under equilibrium conditions, where τ_c is the mean time to hole capture and τ_e is the mean time to hole emission. This is the appropriate initial value for $f_{T\text{-}S}$. Note that $\tau_e/(\tau_e+\tau_c)$ is the average duty cycle for hole trapping: if the hole trap is mostly filled ($\tau_e \to \infty$), it approaches 1; if the hole trap is mostly empty ($\tau_c \to \infty$), it approaches 0. The solution to (3) for the shallow-trap term is therefore

$$f_{T-S}(t) = \frac{T_1}{\left(1+\frac{n_S}{p_h}\right)T_1 + \frac{n_G}{p_h}T_2}\left[1-\exp\left(-\frac{t}{\tau_{NBTI}}\right)\right] + \frac{\tau_e}{\tau_e+\tau_c}\exp\left(-\frac{t}{\tau_{NBTI}}\right) \qquad (4)$$

where $1/\tau_{NBTI} = \sigma v_{th}[(p_h+n_S)T_1+n_G T_2]$. It should be noted that the last term in (4) does not appear in the expression for $f_{T\text{-}D}$ [18]. Based on the Wentzel-Kramers-Brillouin (WKB) approximation, it can be assumed that $T_1 >> T_2$ if the trap is located closer to the channel than to the gate. Since $n_s = 1/\sigma v_{th}\tau_e$ and $p_h = 1/\sigma v_{th}\tau_c$ [23], the saturated value of $f_{T\text{-}S}$ is simply given by

$$f_{T-S}(t) = \frac{\tau_e}{\tau_e+\tau_c}. \qquad (5)$$

Assuming that the hole traps are located at a distance z from the substrate-oxide interface, $N_0 = (q/(L_{eff}W_{eff}))\cdot\delta(x-(T_{ox}-z))$. The integral for ΔV_H can then be evaluated:

$$\Delta V_H\big|_{t\to\infty} = \frac{q}{L_{eff}W_{eff}C_{ox}}\left(1-\frac{z}{T_{ox}}\right)\frac{\tau_e}{\tau_e+\tau_c} \equiv \Delta V_{RTS}\frac{\tau_e}{\tau_e+\tau_c}. \qquad (6)$$

Note that $\Delta V_{RTS} = (q/(L_{eff}W_{eff}C_{ox}))\cdot(1-z/T_{ox})$ is the expression for the V_{th} shift due to RTS derived in [3] in a different manner, and that $\tau_e/(\tau_e+\tau_c)$ is the average duty cycle for hole trapping. Therefore, the expression in (6) represents the time-averaged value of V_{th} shift due to RTS. Substituting (6) into (1), the total V_{th} degradation due to NBTI is expressed by

$$\Delta V_{th}(t) = \Delta V_{RTS}\frac{\tau_e}{\tau_e+\tau_c} + A\left(1-\exp\left(-\frac{t}{\tau_{NBTI}}\right)\right) + Bt^n \qquad (7)$$

where A and B are constants. In (7), the first term corresponds to shallow traps, the second to deep traps, and the third to interface traps. Considering that actual NBTI measurements of V_{th} *vs.* t can be fitted to the empirical model $V_{th}=C+Dt^n$ [20], the first term is included in C, *i.e.* the effect of RTS is included in NBTI degradation.

The relationship between RTS and NBTI is clarified further by examining the factor $\tau_e/(\tau_c+\tau_e) = 1/(1+\tau_c/\tau_e)$. τ_c/τ_e is dependent on the gate voltage V_g and absolute temperature T, decreasing with V_g and increasing with T [3]:

$$\frac{\tau_c}{\tau_e} = \exp\left(K - \frac{q}{kT}\left[\left(1-\frac{z}{T_{ox}}\right)\Psi_S + \frac{z}{T_{ox}}V_g\right]\right). \qquad (8)$$

where K is a constant and Ψ_S is the channel surface potential. Generally, RTS is measured under normal operating conditions (V_{g0}, T_0) whereas NBTI is measured under accelerated stress conditions ($V_{g0}+\Delta V$, $T_0+\Delta T$), so that one must be careful to account for ΔV and ΔT when correlating the first term in (7) with RTS. This can be done by introducing the concept of an acceleration factor $\alpha(\Delta V, \Delta T)$:

$$\frac{\Delta V_{RTS}}{1+(\tau_c/\tau_e)\big|_{(V_{g0}+\Delta V, T_0+\Delta T)}} \equiv \Delta V_{RTS}\cdot\alpha(\Delta V,\Delta T). \qquad (9)$$

Note that (7) deals with a single-trap RTS with depth z where both ΔV_{RTS} and α are the function of z. Therefore we can expand (7) to include the multiple traps with depths z_i (where i represents the trap number) as,

$$\Delta V_{th}(t) = \sum_i \Delta V_{RTS}^i\cdot\alpha_i + A\left(1-\exp\left(-\frac{t}{\tau_{NBTI}}\right)\right) + Bt^n. \qquad (10)$$

The dependence of τ_c/τ_e on V_g is illustrated in the representative example shown in Fig. 1(a), for which the normal operating conditions are (1.0V, 300K) and the NBTI stress conditions are (2.0V, 400K). It can be seen that $\tau_c/\tau_e = 1$ under normal operating conditions, so that α = 50% for (ΔV, ΔT) = (0V, 0K) in Fig. 1(b). In contrast, $\tau_c/\tau_e \approx 0.01$ under NBTI stress conditions, so that $\alpha \approx 100\%$ for (ΔV, ΔT) = (1.0V, 100K). Thus, under NBTI stress conditions, 100% of ΔV_{RTS} appears as an offset in the NBTI-induced V_{th} shift. However, when the stress is removed, α is decreased to its normal value. This implies that the traps responsible for RTS are also responsible for the NBTI recovery as reported in [21, 22]. Note that Fig. 1 is a sample using z/T_{ox}=0.25 and K=18.35 condition and thus, α also depends on the values of z/T_{ox} and K; small z and large K result in large τ_c/τ_e (since $V_g > \Psi_S$) and hence small α.

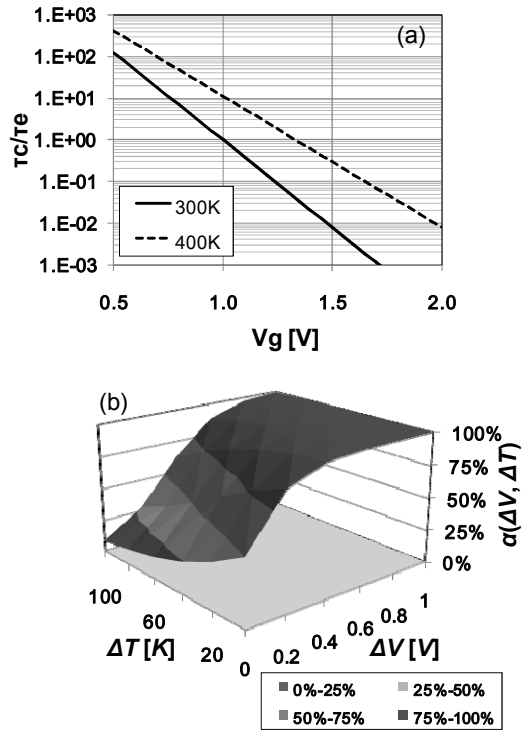

Figure 1: V_g and T dependence of τ_c/τ_e (a) and of the acceleration factor (b). The origin (0,0) in (b) corresponds to the nominal operating condition while (1,100) corresponds to the NBTI stress condition.

III. VALIDATION OT THE THEORY

Both 3-D device simulations using Sentaurus v.2009.06 (Synopsys, Inc.) and measurements of RTS and NBTI-induced V_{th} shifts for pull-up devices in 45nm-node SRAM cells [12] were performed in order to validate the theory as developed above. Fig. 2 shows the 3-D device simulation results for a p-channel MOSFET (L/W = 60nm/60nm, T_{ox} = 2nm) which has a single trap located at the center of the channel area and a distance 0.1nm away from the substrate-oxide interface (z = 0.1nm). The expected dependence of RTS on drain current (I_D) [4] is reproduced, as shown in Fig. 2. Also, the simulated ΔV_{RTS} shows no T dependence (inset), as expected.

Fig. 3 shows the measured dependence of τ_c/τ_e on V_g and T for a pull-up transistor in a 45nm-node bulk-Si SRAM cell. Each τ_c/τ_e data point is extracted from the RTS time-domain measurement. Inset table indicates z/T_{ox} and K values extracted from the slope and y-intercept for 304K and 337K plots, respectively. Those values are almost equivalent to each other, confirming the validity of using (8) at different V_g and T conditions. For instance, since τ_c/τ_e at V_g = 1.1V at 304K is 3.997, we observe 20% of RTS-induced V_{th} shift as the mean-time value at nominal condition. On the other hand, τ_c/τ_e at V_g = 2.0V and T = 400K is evaluated as 1.124E-2, which projects 0.989 of α, *i.e.* 98.9% of the RTS-induced V_{th} shift is expected to be included in the NBTI degradation.

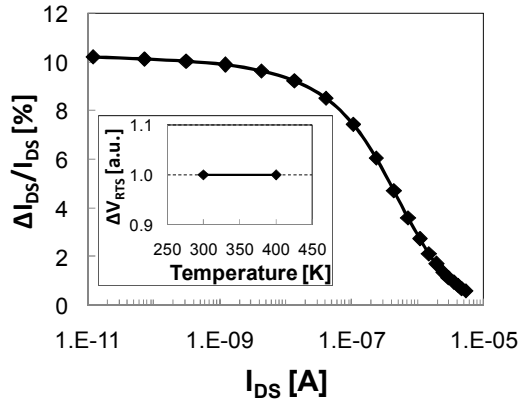

Figure 2: $\Delta I_{DS}/I_{DS}$ dependence on I_D using 3-D device simulation results for a PMOSFET with channel dimensions L/W = 60nm/60nm and uniform body doping $N_{SUB}=10^{18}$ cm^{-3}. Inset shows temperature dependence of ΔV_{RTS}.

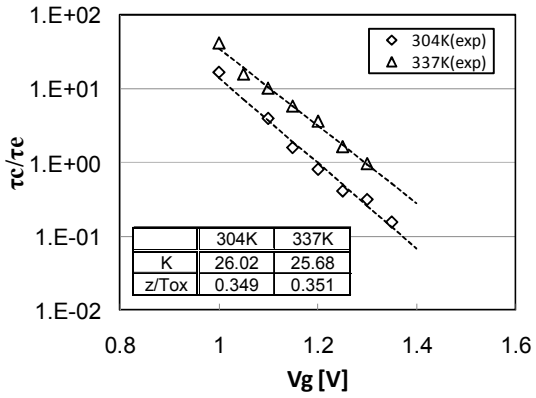

Figure 3: Measured V_g and T dependence of τ_c/τ_e, for a pull-up transistor within a 45nm-node bulk-Si SRAM cell.

Fig. 4(a) shows measured V_{th} degradation at $|V_g|$= 1.5V and T = 400K using the on-the-fly (OTF) technique [24, 25]. A prior work reveals that the hole trap effect saturates within 1-s after stress, while the interface trap component starts degrading after 1-s [26]. Based on this fact, V_{th} degradation during the first second can be entirely attributed to RTS with no interface trap effect. Fig. 4(b) is a close-up graph of Fig 4(a), and it also shows the RTS observed at V_g = 1.1V, T = 300K. Note that (i) the RTS was measured for about 20 sec using the alternating bias method [12], where the time axis is normalized to 1-s scale duration to compare the amplitudes, (ii) the ΔV_{th}=0 point (bottom line of RTS data) is being shifted upward. From this graph, NBTI behavior can be separated into three phases; first, there is a deep trap effect that appears in the second term of (10) as well as in the fluctuation (Phase 1). Second, there appears the RTS related fluctuation with an amplitude equivalent to that observed at the nominal condition (Phase 2). A rough estimate of the acceleration factor α from the phase 2 is 57%, compared to 23% for the nominal operating condition, confirming that α is larger for higher V_g and T. Third, additional RTS fluctuations appear with amplitudes of ~3mV and ~5mV in arbitrary units (a.u.),

equivalent to those observed in Phase 1, by subtracting out the deep trap effect (Phase 3). In summary, for V_{th} degradation due to NBTI, a deep-trap effect appears during the first 1-s of stress, then RTS (with larger α value than observed for the nominal operating condition) appears, followed by some additional RTS induced by the NBTI stress.

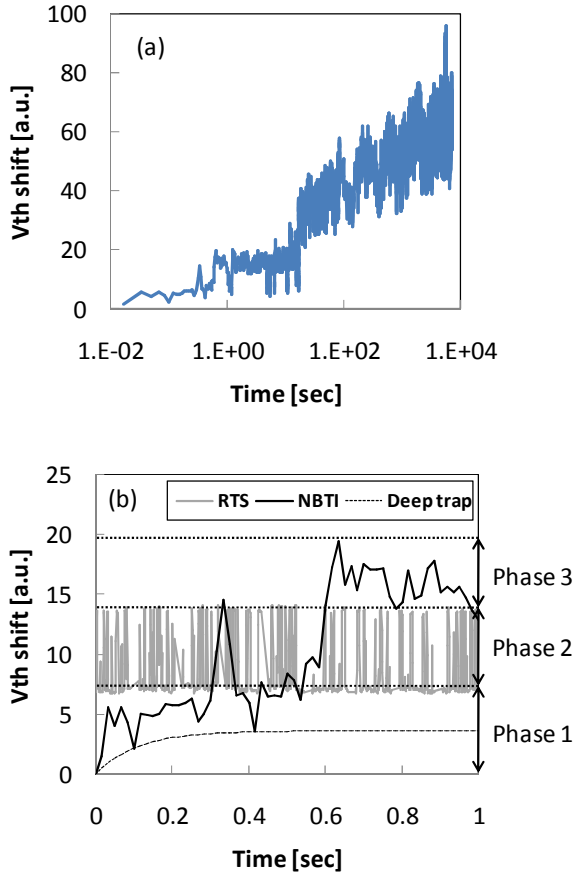

Figure 4: V_{th} degradation under NBTI stress for long time (a), for 1s after stress (b). In (b), the gray line is the RTS observed for nominal bias condition. Black dashed line indicates deep trap effect which is obtained by fitting $A(1\text{-}\exp(-t/\tau_{NBTI}))$ to the local minimum points.

Figure 5(a) shows the V_{th} shift induced by NBTI for long stress times (from 5000 sec to 7200 sec in Fig. 4(a)) using a time lag plot (TLP) developed by T. Nagumo *et al.* [27], which was originally used for analyzing RTS. In this method, based on a sequence of V_{th} shifts represented by x_i (i=data number), we generate a two dimensional variable (x_i, x_{i+1}) and plot it on the x-y plane. We use the TLP because it allows us to analyze the RTS amplitude more effectively than using a complex time-domain waveform. Since the NBTI-induced V_{th} shift includes a time-dependent component associated with the interface trap, the data distributes toward the upper right-hand side compared with the case of RTS analysis [27]. From this figure, three diagonal trend lines can be identified. The difference between those lines is found to be 7mV (a.u.) and corresponds to the RTS amplitude observed in the NBTI degradation. To see this more effectively, we extract the absolute values of all points measured from the diagonal line in Fig. 5(a) (see Fig. 5(b)). A peak at 7mV is observed as well as at 5mV, which is related to the RTS observed in Phases 1 and 3 as discussed with regard to Fig 4(b). Regarding the RTS with 3mV amplitude, it is hard to distinguish a peak in this graph; however, it is noticeable that some large V_{th} shifts with ~15mV are observed, which can be explained by coincident RTS with amplitudes of 7, 5 and 3mV. Therefore, RTS observed during the first 1s of NBTI degradation is retained for long stress times, showing the validity of equation (10).

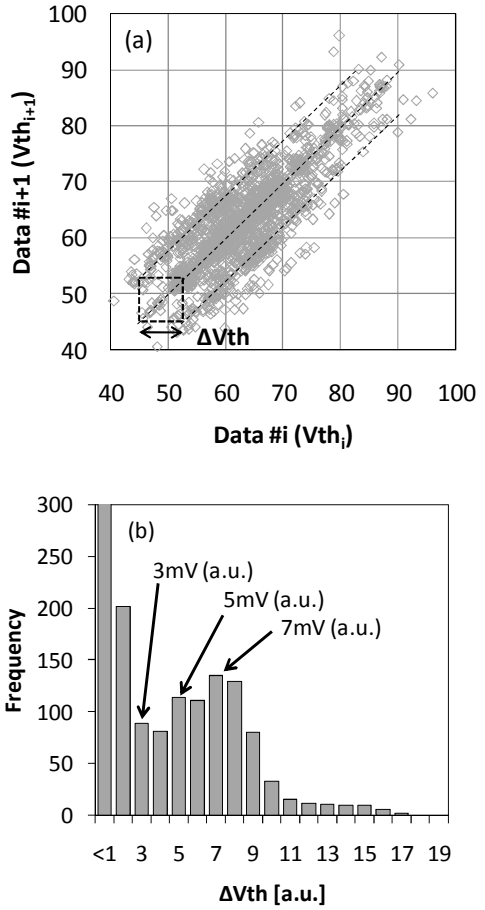

Figure 5: V_{th} degradation of NBTI during 5000 s to 7200 s stress time using TLP metric (a) and the distribution of amplitudes extracted from the diagonal line (b).

To compare the RTS and NBTI data more quantitatively, it is effective to take the time-averaged V_{th} shift after 1 sec stress because the first and the second terms in (10) represent the time-averaged amplitude. Regarding Fig. 4(b), we obtain 10.15mV (a.u.) for NBTI and 2.07mV (a.u.) for RTS, indicating that the time-averaged V_{th} shift of NBTI has a larger value than that of RTS. We performed the same experiment for multiple transistors in our chip and compared the time-averaged V_{th} shift of RTS with that of NBTI (see Fig. 6). All points appear above the diagonal line, confirming that the RTS-induced shift is included in the NBTI-induced shift, validating the theory developed in this work.

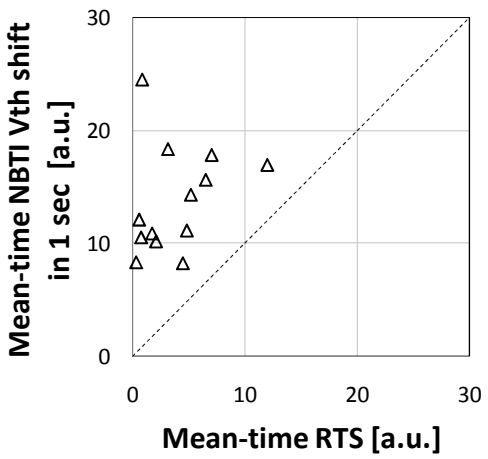

Figure 6: Comparison between mean-time V_{th} shift of RTS and that of NBTI during 1 sec after applying stress.

IV. CONCLUSION

The expression for the V_{th} shift due to RTS is derived starting from a well-known model for V_{th} degradation due to NBTI. This indicates that the hole traps primarily responsible for the time-independent V_{th} shift (modeled by the mean-time V_{th} shift during 1 sec after stress) under NBTI stress are the same ones responsible for RTS. The mean-time V_{th} shift of NBTI during 1 sec that is manifested as RTS, referred to herein as an acceleration factor α, is dependent on the NBTI stress conditions (gate voltage and temperature). 3-D device simulations and SRAM pull-up transistor measurements are consistent with this theory. It can be concluded, therefore, that adding design margin for RTS independently of the design margin for NBTI would result in overly conservative VLSI design.

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