A 2-Gb/s 5.6-mW Digital Equalizer for a LOS/NLOS Receiver in the 60GHz Band

Ji-Hoon Park, Brian Richards, and Borivoje Nikolić
Electrical Engineering and Computer Sciences, University of California at Berkeley

***Abstract*- The wide unlicensed bandwidth of a 60GHz channel presents an attractive opportunity for high data rate and low power personal area networks (PANs). The use of single-carrier modulation is beneficial for efficient transmitter and receiver implementation. Equalization of the long channel response in non-line-of-sight (NLOS) conditions presents a significant challenge. A digital equalizer for 60GHz channels has been designed for both line of sight (LOS) and NLOS channel conditions based on the IEEE WPAN standard. Power consumption is minimized by using parallelized distributed arithmetic (DA). A 2mm x 2mm test chip in 65nm CMOS implements a 6-tap feedforward and 32-tap feedback equalizer that consumes 5.6mW at 2.0Gb/s throughput.**

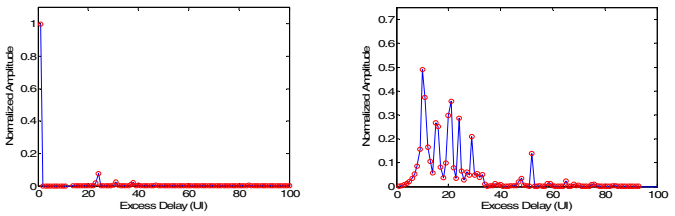
I. INTRODUCTION

The 7GHz of unlicensed bandwidth at 60GHz is very attractive for high rate video and data transfers. Current developments are focused on uncompressed high-definition video transfer indoors between a set-top box and a display. These systems mitigate long channel impulse response by using OFDM modulation [1],[2], consuming relatively high power, which is not seen as a problem for wall-plugged devices. The wide bandwidth available in the 60GHz band also presents an opportunity for high-speed links between portable devices, where in addition to video transfer, potential applications include high-rate data transfers between mobile devices. To improve the power amplifier efficiency, this system is expected to utilize a single-carrier constant-envelope modulation scheme.

The main challenge for a high data rate receiver in the 60GHz band is the need to equalize a very long channel response, which causes an inter-symbol interference (ISI) of several tens of symbols [3]. Fig.1 shows examples of the impulse responses generated from the IEEE channel model for LOS and NLOS conditions [4]. Phased-array transmitters and receivers have been developed for reducing the multipath propagation [5]. In order to achieve a low power consumption of the receiver, an analog equalizer has been explored [6]. However, reported solutions so far implement only a small number of taps suitable for LOS propagation conditions.

As an alternative, high delay spread channel equalizers for DTV, WiFi and cellular systems have been implemented using digital signal processing techniques.

In this paper, we propose a fully digital baseband receiver for a single carrier 60GHz transceiver that can operate in both LOS and NLOS conditions. The resulting chip implements an all-digital equalizer and channel estimator (CE). To simplify the test procedure, a transmitter with a channel emulator and noise generator is embedded.



(a) (b)

Figure 1. Channel impulse responses (h_m) examples from the IEEE model (a) LOS (CM1.4), (b) NLOS (CM2.3) [4].

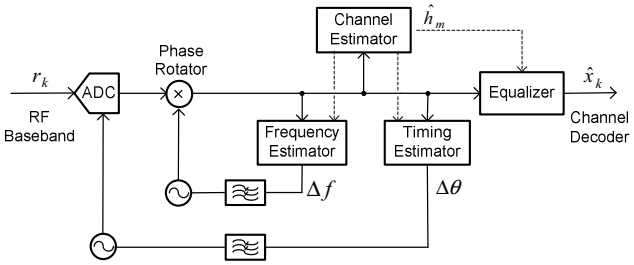


Figure 2. General digital receiver baseband.

In the section II, the high-level architecture of the receiver is explained. The equalizer structure is described in the section III, followed by the channel estimation in the section IV. The measurement results from the implemented chip will be given in the section V with the conclusion drawn in the section VI.

II. SYSTEM

A. Modulation Scheme

This work implements the single-carrier modulation option from the amended IEEE WPAN standard [4]. This standard includes both OFDM and single-carrier modulation options. While OFDM has its advantages in relative immunity to multipath propagation, it results in higher system power. On the transmit side, the high peak-to-average ratio (PAR) of the OFDM signal requires back-off in the power amplifier to maintain linearity. On the receive side, high resolution ADC and FFT blocks must be operated regardless of the channel conditions. Finally, it is generally hard to vary the channel coding adaptively in an OFDM system.

BPSK modulation is chosen for the implementation to simplify the design. However, an extension to QPSK can be easily done by duplicating and slightly modifying the data path. Higher-order modulation such as 16QAM does not benefit from equalization, because in the NLOS channels, the required signal-to-noise ratio (SNR) often cannot be achieved even with an ideal equalizer.

978-1-4244-8298-6/10/$26.00 ®2010 IEEE

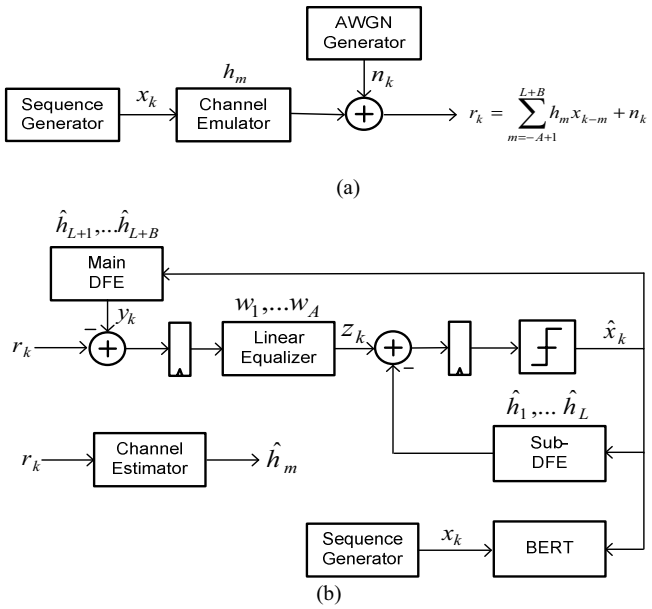


Figure 3. Implemented blocks (a) transmitter, (b) equalizer and channel estimator.

Fig.2 shows a general digital baseband for a single-carrier system consisting of an ADC, a channel estimator, timing and frequency estimators with correction paths, and an equalizer block.

B. Receiver Structure

The implemented test chip contains the blocks shown in Fig.3. The receiver consists of an equalizer and a channel estimator, which estimate the channel impulse response using a pilot sequence, which can be used for the frequency and timing error detection as well as the coefficient calculation for the equalizer. For testing purposes, the transmitter, the channel emulator, and the noise generator, are implemented as well. A configuration scan chain, debug logic, and an equalizer memory initialization are provided as well to facilitate the chip verification from an external test FPGA.

III. EQUALIZER

The main objective is to design a NLOS equalizer that enables a 2Gb/s throughput with minimum power consumption.

A. Reduced Complexity Equalizer Structure

There are numerous options for implementing a complex equalizer. The frequency domain equalizer has been excluded from consideration because it has high power consumption similarly to the OFDM receiver. The implemented equalizer in Fig. 3b. is a hybrid, consisting of a linear equalizer (LE) and two decision-feedback equalizers (DFEs), the main DFE (M-DFE) and the sub-DFE (S-DFE). To minimize the noise enhancement characteristic of LEs, a LE with a limited number of taps (A) is used to cancel the pre-cursor.

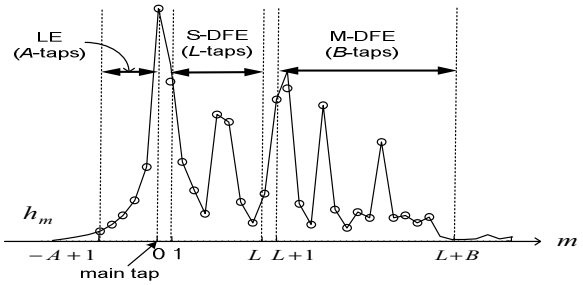


Figure 4. Tap assignment of the equalizer.

Despite its error propagation problem, the decision feedback equalizer (DFE) has been a popular solution for single carrier systems because of its low hardware complexity. Unlike conventional LE-DFE structure, DFE output is fed back to the input of the LE (Fig.3b), by which the channel estimation output can be directly used for the DFE coefficients, thereby significantly reducing the number of operations [7]. Also, with this structure, the DFE taps can be implemented in either the analog and digital domains, for further power optimization.

In addition to the main DFE (M-DFE), the sub-DFE (S-DFE) is included to compensate for the latency of the loop by limiting the feedback delay to one symbol period. Fig.4 shows the tap assignment of each equalizer element for an impulse response.

Fig.5a shows the floating and fixed point BER equalizer performance for AWGN and the NLOS channel from Fig.1b. Based on simulation results for various channel scenarios, the numbers of filter taps were decided to be A=6, B=24, and L=8.

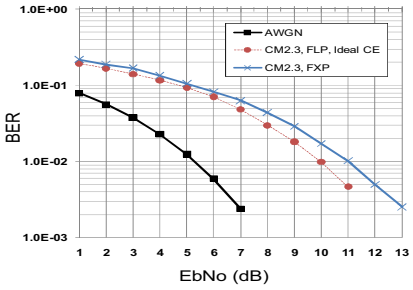


Figure 5. Link-level simulation results with the equalizer.

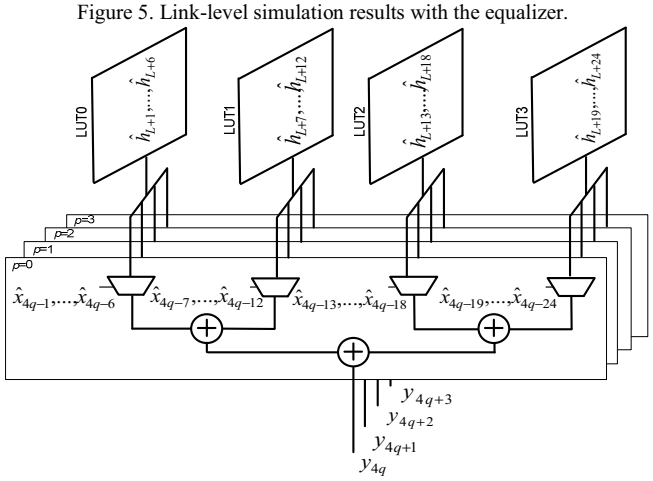


Figure 6. M-DFE (4-way parallelized, 24-tap DA FIR with 4-LUTs).

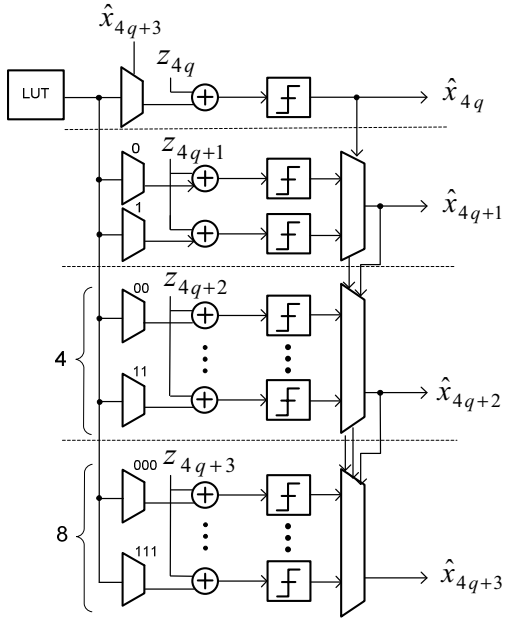


Figure 7.S-DFE (loop-unrolled, 8-tap DA FIR with a LUT).

B. Hardware Implementation

The equalizer is divided into four parallel datapaths to meet the throughput requirements with low power consumption. For the FIR component of the LE and M-DFE, the DA architecture is chosen to reduce the latency. The architecture replaces multiply-and-add operations with the pre-computed look-up tables (LUT) [8]. In this particular implementation, we put emphasis on shortening the latency to meet the timing requirement of the feedback loop.

Fig.6 illustrates the M-DFE implementing the 24-tap FIR

$$y_k = \sum_{m=1}^{24} \hat{h}_{L+m} \cdot \hat{x}_{k-m} \quad (q \in Z) \qquad (1)$$

which can be parallelized as

$$y_{4q+p} = \sum_{m=1}^{24} \hat{h}_{L+m} \cdot \hat{x}_{4q+p-m} \quad (p = 0,1,2,3)\,. \qquad (2)$$

From (2), the filter can be implemented with four identical blocks and a time-shifted input delay line. Each of the blocks is implemented by the summation of the output of four LUT, which can be expressed as

$$\begin{aligned} y_{4q+p} = {} & \sum_{m=1}^{6} \hat{h}_{L+m} \cdot \hat{x}_{4q+p-m} \quad + \\ & \sum_{m=7}^{12} \hat{h}_{L+m} \cdot \hat{x}_{4q+p-m} \; + \\ & \sum_{m=13}^{18} \hat{h}_{L+m} \cdot \hat{x}_{4q+p-m} \; + \\ & \sum_{m=19}^{24} \hat{h}_{L+m} \cdot \hat{x}_{4q+p-m}\,. \end{aligned} \qquad (3)$$

Without optimization, sixteen different memory instances would be required to implement the filter in (3). However, because the LUTs share the same contents, they can be implemented with four multi-ported memories. In this implementation for M-DFE, the LUTs with 64 words are built with D-FFs and MUXs as shown in Fig.6. The LE and the channel emulator also share the same architecture with 6-LUTs (64 words) and 12-LUTs (72-taps, 64 words), respectively,

The S-DFE structure is different because it has to implement a single-cycle feedback, which would be impossible in a conventional parallel structure. Therefore, S-DFE is combined with the slicers and loop-unrolled [9] and then implemented in a DA manner. This 8-tap filter needs only one LUT (Fig.7).

MUXs are added to the delay line to enable adjustable tap allocation, which makes it possible to configure the equalizer to cancel ISI as long as 72 taps away.

In the implementation, the coefficients of the equalizer filters are calculated based on the channel estimation results. The coefficients of the feedforward equalizer ($\boldsymbol{w}$) can be calculated using a MMSE criterion or frequency domain inversion [7]. The complexity of this operation is low because there are only six taps for the LE.

As shown in Fig.5, the BER performance degradation caused by the CE error is less than 1-dB under common operating conditions.

IV. Channel Estimator

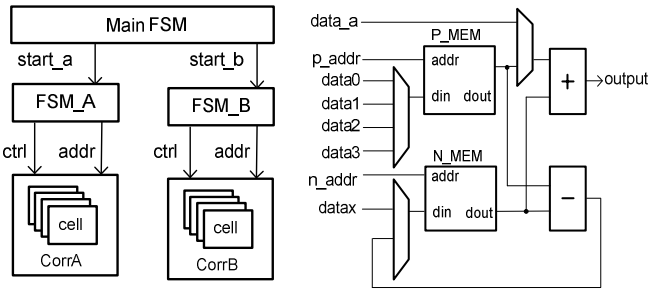
The IEEE WPAN standard specifies channel estimation sequences based on Golay codes, both in a preamble (PCES) and within data bursts (TS) [4]. The Golay correlator can be implemented as a pulse compressor and require an order of magnitude fewer operations than a PN sequence correlator [10].

Fig.8 shows the block diagram of the channel estimator with a parallelization factor of four, which is chosen mainly because of the datapath compatibility with the equalizer. The estimator is designed in such a way that different parallelization factors can be easily accommodated.

The shifting operation required in the correlator is implemented by the manipulation of the buffer address when the shifting value is a multiple of the parallelization factor. When the shifting value is a fraction of the parallelization factor, the operation is implemented by introducing the swap and selective shift operation.

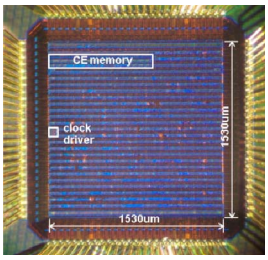
The channel estimation within the data burst can be done using the same hardware, which can be used for frequency and timing error detection.

V. Measurement Results

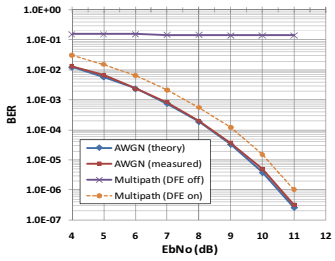


(a) (b)

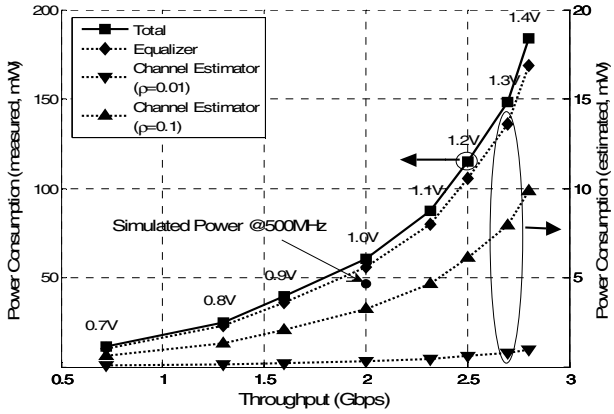
Figure 8.Channel estimator architecture (a) block diagram, (b) cell structure.



(a)



(b)



(c)

Figure 9. Chip implementation, (a) photo, (b) measured BER performance, (c) power and throughput.

The chip was synthesized using a customized design flow [11] and fabricated by TSMC in 65nm CMOS. Although the core size of the chip is 1.53mm by 1.53mm, the design is pad-limited with a utilization factor of 15.1%. The chip photo is shown in Fig.9a.

Fig.9b shows the measured BER performance for both an AWGN and a multipath channel, verifying the correct operation. The deviation from the theoretical performance shows the effect of the error propagation in the DFE.

Fig.9c shows the measured total power consumption with varying throughput. As shown in the figure, the post-synthesis estimated power consumption of 46.7mW is close to the measured 60.7mW at 2Gb/s. The power breakdown derived from the synthesis estimates is adjusted proportionally to estimate the actual power consumption of each block. Because the channel estimator is only active during the preamble period, a duty cycle, ρ, scales the result.

VI. Conclusion

A digital signal processing chip that can equalize a high-delay spread channel seen in NLOS conditions at the 60GHz band is presented. An equalizer minimizes the power consumption by using the parallelized DA architecture. A configurable 38-tap equalizer can be implemented with 5.6mW power consumption with 2Gbps throughput. A channel estimator for calculating the equalizer coefficient and measuring the synchronization error is also developed based on the IEEE WPAN standard. The power consumption of the proposed architecture might be further reduced by implementing a part of it in a mixed signal domain.

	[12]	[6]	This work
Technology	0.25um CMOS	90nm CMOS	65nm CMOS
Data rate	2Gbps	1Gbps	2Gbps
Number of taps	2-tap DFE	16-tap DFE	6-tap LE 32-tap DFE
Power	10mW	14mW	5.6mW

Table 1. Comparison to prior works

Technology	TSMC 65nm CMOS	
Supply	1.0V (core), 2.5V (IO)	
Chip area	2 mm x 2mm	
Throughput	0.72Gbps (@180MHz)~ 2.8Gbps (@700MHz)	
Power dissipation (multipath, EbNo=4dB)	Total	11.1mW (@0.72Gbps) 60.7mW (@2.0Gbps) 183.8mW (@2.8Gbps)
	Equalizer (estimated)	5.6mW (@2.0Gbps)
	CE (estimated)	3.3mW (@2.0Gpbs, $\rho = 0.1$)

Table 2. Chip summary

Acknowledgments

The authors wish to acknowledge the support of the Samsung Scholarship, the C2S2 Focus Center, one of six research centers funded under the Focus Center Research Program (FCRP), a Semiconductor Research Corporation entity, and TSMC University Shuttle Program for the fabrication of this design. The authors also would like to thank Kwangmo Jung for the clock driver design and appreciate the contributions of students, faculty and member companies of the Berkeley Wireless Research Center.

References

[1] WiMedia Alliance, http://www.wimedia.org/
[2] SiBeam Inc., http://www.sibeam.com/
[3] H. Xu, V. Kukshya, and T.S. Rappaport, "Spatial and temporal characteristics of 60-GHz indoor channels," *IEEE J. Selected Areas in Communications,* vol. 20, pp.620-620, Mar. 2002.
[4] IEEE WPAN milimeter wave alternative PHY task group 3c (TG3c).
[5] S. Reynolds et al., "A 16-element phased-array receiver IC for 60-GHz communications in SiGe BiCMOS," *Symp. RFIC Dig.* 2010.
[6] D. Sobel and R.Brodersen, "A 1Gbps mixed-signal analog front-end for a 60GHz wireless receiver," *Symp.VLSI Circuits Dig.,*pp.156-157, 2008.
[7] I.J. Fevier, S.B. Gelfand, and M.P. Fits, "Reduced complexity decision feedback equalization for multipath channels with large delay spreads," *IEEE Trans. on Comm.*, vol. 47, pp. 810-816, Jun. 1999.
[8] S.A.White, "Applications of distributed arithmetic to digital signal processing: a tutorial review," *IEEE ASSP Magazine*, vol.6, pp. 4- 19, Jul. 1989.
[9] V. Stojanovic et al.,"Autonomous dual-mode (PAM2/4) serial link transceiver with adaptive equalization and data recovery," *IEEE J. Solid-State Circuits,* vol. 40, no. 4, pp. 1012-1025. Apr. 2005.
[10] B.M. Popovic, "Efficient Golay correlator," *Electonics Letters*, vol.35, No. 17, pp. 1427-1428, Aug. 1999.
[11] D. Markovic, C. Chang, B. Richards, H. So, "ASIC design and verification in an FPGA environment," *Proceedings of CICC*, pp. 737-740, Sep. 2007.
[12] S.J. Bae et al., "A 2Gb/s 2-tap DFE receiver for multi-drop single-ended signaling systems with reduced noise," *ISSCC Dig. of Tech. Papers,* pp. 244-245, Feb. 2004.