SRAM Yield Enhancement with Thin-BOX FD-SOI

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Abstract

The performance and yield of 6-T SRAM cells implemented in thin-BOX FD-SOI technology *vs.* bulk technology are compared via 3-dimensional (3D) atomistic process and device simulations and analytical modeling for SRAM yield estimation. Performance is enhanced due to the elimination of channel dopants, and variation due to gate-LER and RDF are suppressed, for FD-SOI technology. For the same cell area (~0.07μm^2), comparable SNM can be achieved with 30% higher write current, and SRAM yield is enhanced by >2 sigma.

Introduction

Continued bulk MOSFET and SRAM cell area scaling are becoming increasingly difficult due to increased random variation in transistor performance with decreasing gate length (L_{GATE}), caused by gate line-edge roughness (LER) and random dopant fluctuations (RDF) [1]. The use of a lightly doped (fully depleted) SOI MOSFET structure with a thin (~10 nm-thick) buried oxide (BOX) and a heavily doped substrate has been reported to be effective for suppressing this variation [2]. The thin-BOX structure (*vs.* a thick-BOX structure) has been shown to be optimal for SRAM in sub-50nm technology nodes [3]. In this work, the benefits of thin-BOX FD-SOI technology *vs.* bulk MOSFET technology for improving 6-T SRAM cell yield at the 22nm technology node are assessed, via 3-dimensional (3D) atomistic process and device simulations and analytical modeling for SRAM yield estimation.

Thin-BOX FD-SOI MOSFET Design

Fig. 1a shows a cross-sectional view of an n-channel thin-BOX FD-SOI MOSFET structure simulated in this work. Device parameters are summarized in **Table I**, and were selected according to [4] for superior short-channel effect control and to allow for effective back-biasing. The structure is fabricated using an implantation-free process to avoid dopant straggling and damage-induced defects in the thin body region [4], to reduce RDF-induced variations. The process uses a low-temperature, zero-silicon-loss epitaxial growth process to form (faceted) *in-situ*-doped (10^{20} cm^{-3}) raised-source/drain regions – from which dopants are diffused to form the lightly doped source/drain extensions – to reduce series resistance with minimal increase in sidewall gate capacitance [4]. The gate work function (Φ_M) was selected to achieve the LOP ITRS specification for off-state leakage current (I_{OFF}), ~3nA/μm. For comparison, planar bulk MOSFETs with uniform channel doping profile (10^{18} cm^{-3} boron), doped poly-Si gate (Φ_M= 4.05eV), and comparable I_{OFF} were also simulated. **Fig. 2** shows the transfer characteristics for n-channel FD-SOI and bulk MOSFETs. The FD-SOI MOSFET exhibits steeper sub-threshold slope (due to negligible depletion capacitance) and higher drive current (due to higher carrier mobility). **Table II** provides a summary comparison of device performance parameters. A simple analytical model was fit to the simulated current-voltage data (Fig. 2), to allow for fast estimation of SRAM metrics such as read static noise margin (SNM) [5] and write current (I_w) [6].

Variation Analysis

Variation in transistor threshold voltage (V_{TH}) due to RDF was evaluated using 3D Kinetic Monte Carlo (KMC) simulations (100 cases for each nominal design), which include reactions between defects and impurities as predicted by molecular dynamics. As shown in **Fig. 3**, $\sigma(V_{TH})$ is reduced (by more than 50%) for the FD-SOI structure because of the elimination of dopants within the channel region.

100 different gate line profiles were derived from a scanning electron microscopy image of photoresist lines processed for the 22nm node, and were used to define gate electrodes with realistic LER for 3D device simulations. The $\sigma(V_{TH})$ values extracted from these simulations are summarized in Fig. 3. Due to reduced short-channel effects, the FD-SOI structure provides for smaller LER-induced variation. Assuming that LER and RDF are independent process variables, the total random variations are estimated to be $\sigma(V_{TH})|_{SOI}$ = 23mV, $\sigma(V_{TH})|_{BULK}$ = 51mV.

6-T SRAM Cell Design

The 22nm-node SRAM cell (**Fig. 1b**) dimensions summarized in **Table III** were selected based on recent publications [7-11]. **Figs. 4a and 4b** show the butterfly plots and N-curves for each structure, respectively, obtained using the analytical model. Although the SNM is slightly lower (by 10%) due to a lower nominal $|V_{TH}|$ values, I_w is 71% higher for the FD-SOI cell. For a fixed cell area (~0.07μm^2), comparable SNM values (~207mV) can be achieved by decreasing the widths of the pass-gate transistors (W_{PG}) in the FD-SOI cell, in which case I_w for the FD-SOI cell (~14μA) is still 30% higher than that for the bulk cell (~ 11 μA). **Figs. 4c and 4d** show the dependencies of SNM and I_w on V_{DD}, respectively. It can be seen that the FD-SOI cell provides for higher I_w at comparable SNM over the entire range of V_{DD} values.

SRAM Yield Estimation

The concept of cell sigma, defined as the minimum amount of variation for read/write failure [12], is used to assess SRAM yield. Random variations due to gate-LER and RDF, as well as global (Gaussian) variations due to process-induced variations in L_{GATE} and channel width (±10%) are considered. **Fig. 5** shows that the minimum V_{DD} (meeting six-sigma yield) is ~0.6V for the FD-SOI cell. In contrast, the bulk cell cannot meet the six-sigma yield requirement for any value of V_{DD}; it achieves only 4-sigma at V_{DD} = 0.8V.

Conclusion

The performance and yield of 6-T SRAM cells implemented in thin-BOX FD-SOI technology *vs.* bulk technology are compared. Performance is enhanced due to the elimination of channel dopants and variation due to gate-LER and RDF are suppressed for FD-SOI technology. This results in improved write current and higher cell sigma for FD-SOI technology. Therefore, thin-BOX FD-SOI is promising for continued 6-T SRAM cell area scaling.

Acknowledgements

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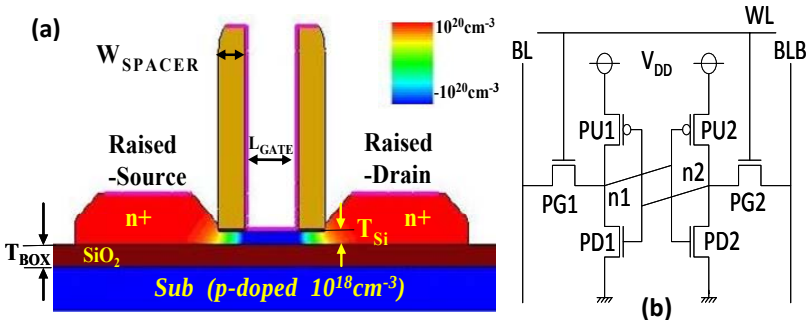


Fig. 1. (a) Cross-sectional view of the thin-BOX FD-SOI MOSFET, **(b)** Circuit schematic of the 6-T SRAM cell.

Table I. FD-SOI device parameters

Parameter	Value
L_{GATE}	25nm
L_{eff}	35.6nm
W_{SPACER}	15nm
T_{OX}	1nm
T_{BOX}	10nm
T_{SI}	6nm
Φ_M	4.45eV

Table II. Comparison of device performance: V_{DD}=1.0V

	FD-SOI	Bulk
I_{ON} [μA/μm]	861	581
I_{OFF} [nA/μm]	3	3
SS [mV/dec]	75	81
$V_{T,LIN}$ [mV]	160	166
$V_{T,SAT}$ [mV]	114	120
DIBL [mV/V]	51	51

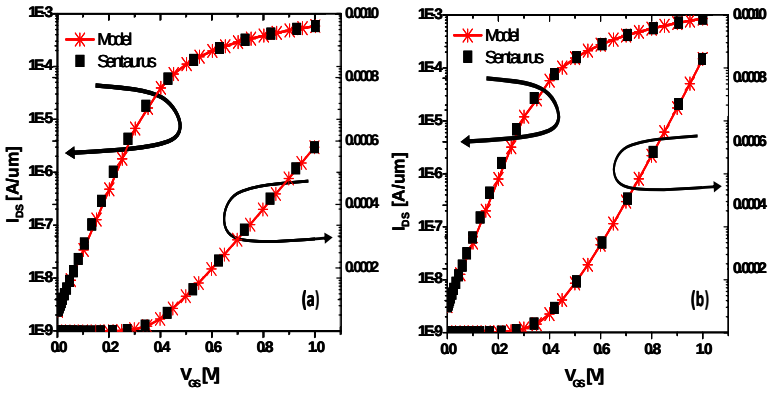


Fig. 2. Comparison of I_{DS}-V_{GS} (V_{DS}=V_{DD}=1.0V) curves of **(a)** Bulk **(b)** FD-SOI. The fitted curves are matched within 5%. An analytical short-channel *I-V* equation was fit to 6 different current values from Sentaurus, for (V_{GS}, V_{DS}) = {(1.0, 0.1), (1.0, 1.0), (0.5, 1.0), (1.0, 0.5), (0.0, 1.0), (0.5, 0.1)} [12].

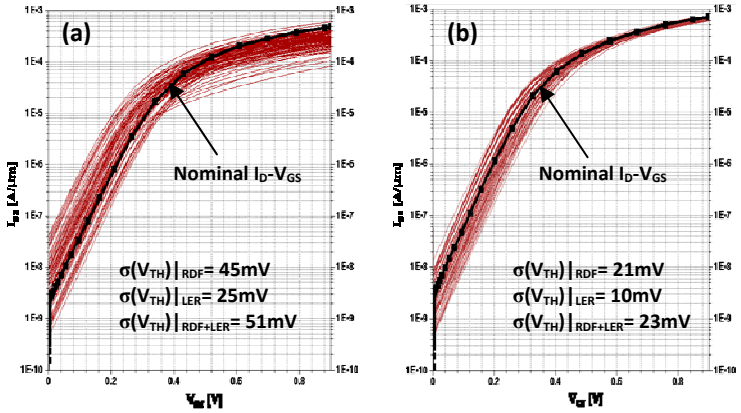
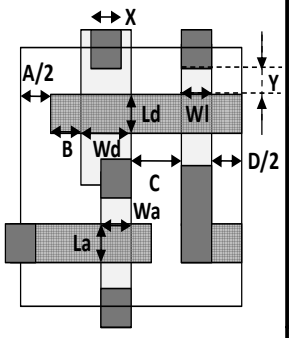
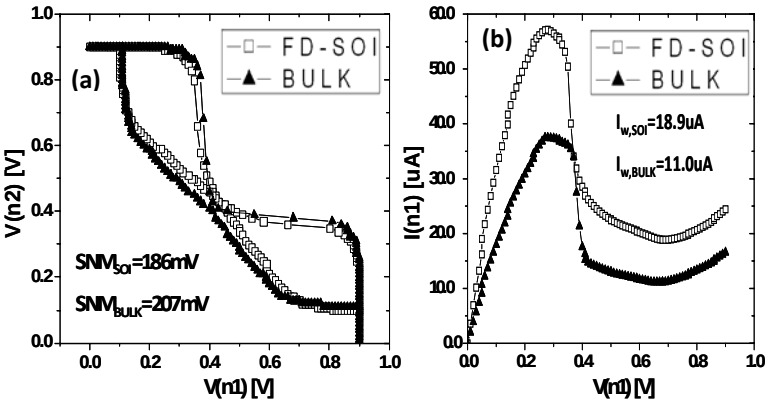


Fig. 3. Atomistic simulations of I_{DS}-V_{GS} of **(a)** Bulk **(b)** FD-SOI. Due to the elimination of channel doping, $\sigma(V_{TH})$ is dramatically suppressed for FD-SOI. Note that variation induced by gate-LER results in smaller $\sigma(V_{TH})$. V_{DD}=0.9V.

Table III. FD-SOI 6-T SRAM cell dimensions: A half-bit cell image is shown on the left side below.



Design rules		Symbol	Size [nm]
Cell Height	PG CH length	La	25
	PD CH length	Ld	25
	CONT size	X	30
	Gate-to-CONT	Y	20
	Total	190	
Cell Width	POLY-to-POLY	A	30
	POLY-to-DIF ext	B	20
	PD Width	Wd	55
	N/P isolation	C	50
	PU Width	Wl	32
	DIF-DIF (min)	D	50
	Total	394	
A SRAM cell area		0.07486 μm²	



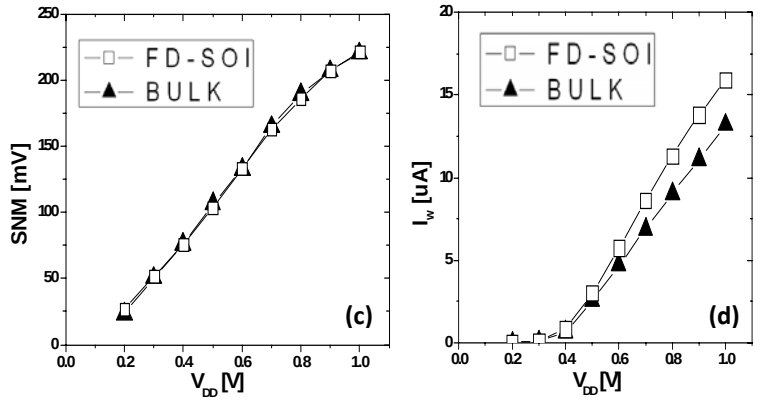


Fig. 4. Comparison of **(a)** Static Noise Margin **(b)** and the write current, for V_{DD}=0.9V. The write-ability of the FD-SOI SRAM cell improved by 71%, with 10% lower SNM. For **(c,d)**, 28.5nm W_{PG} in the FD-SOI SRAM cell is used to achieve comparable SNMs.

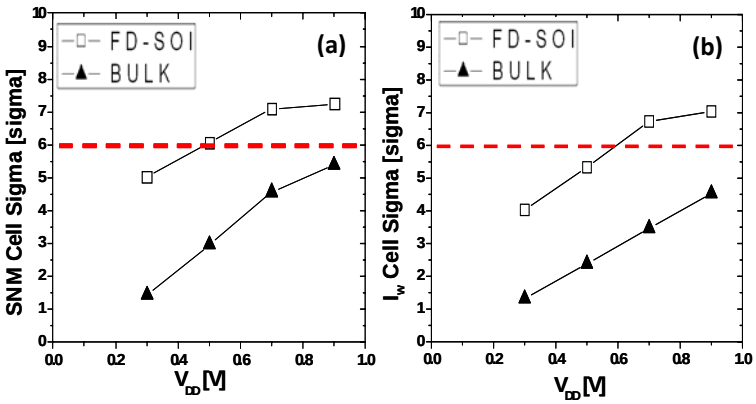


Fig. 5. Comparison of the cell sigma for **(a)** SNM **(b)** and I_w.