SRAM Cell Design Considerations for SOI Technology

*[1]Tsu-Jae King Liu, [1]Changhwan Shin, [1]Min Hee Cho, [1]Xin Sun, [1]Borivoje Nikolić, and [2]Bich-Yen Nguyen
[1]Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720 USA
[2]SOITEC, 1010 Land Creek Cove, Austin, TX 78746 USA
*Phone: +1-510-643-9251, Fax: +1-510-642-2739, E-mail: tking@eecs.berkeley.edu

Abstract

The performance and threshold-voltage variability of vertical SOI FinFETs are compared against those of planar fully depleted SOI MOSFETs with thin buried oxide, via three-dimensional device simulation with atomistic doping profiles and gate line-edge roughness, for the 22 nm CMOS technology node (25 nm gate length). Compact modeling is then used to estimate six-transistor SRAM cell performance metrics. Although FinFET technology offers superior performance, it is projected to have lower yield for comparable cell area, due to higher sensitivity to random and process-induced variations.

Introduction

Increasing variation in transistor performance with miniaturization is a major challenge for continued bulk/PD-SOI CMOS technology advancement [1,2]. In particular, random variations in threshold voltage (V_{TH}) due to gate line-edge roughness (LER) and random dopant fluctuations (RDF) will increase significantly as the gate length (L_G) is scaled down below 30 nm [3]. Increased transistor mismatch results in lower SRAM cell yield, and hence threatens to limit cell-area scaling and/or operating voltage (V_{DD}) reduction. Advanced transistor structures which suppress short-channel effects more effectively than conventional bulk/PD-SOI MOSFET structures, without the need for heavy channel doping, likely will be needed to overcome this challenge for sub-22 nm CMOS technology nodes.

The FinFET [4] offers the improved electrostatic integrity of a double-gate MOSFET structure and has a process flow and layout similar to that of the conventional MOSFET [5]. In order to effectively suppress short-channel effects (SCE), the thickness of the body (*i.e.* the fin width) should be no greater than 2/3 times the gate length (L_G) [5]. In order to minimize RDF effects, the body should be undoped [6]. Fin LER can be an issue, but can be mitigated by using spacer lithography [7]. Six-transistor (6-T) SRAM cells fabricated with FinFETs have been reported to achieve improved performance for comparable write and static noise margins, as compared with cells fabricated with planar MOSFETs [6].

The planar FD-SOI MOSFET structure with a very thin (~10 nm-thick) buried oxide (BOX) layer and a heavily doped substrate has been shown to be effective for reducing the impact of parameter variations and RDF, due to its excellent electrostatic integrity and the elimination of body doping [8]. Recently, functional SRAM cells were demonstrated using such FD-SOI devices, for the 32 nm technology node and beyond [9].

In this paper, SOI FinFET and thin-BOX planar FD-SOI MOSFET technologies are compared with regard to 6-T SRAM cell performance and yield, at the 22 nm technology node, via three-dimensional (3D) atomistic process and device simulations with advanced physical models [10], and analytical modeling for SRAM yield estimation.

SOI MOSFET Designs

The transistor designs considered herein have undoped body regions and were optimized for a gate length (L_G) of 25 nm and equivalent gate-oxide thickness (T_{ox}) of 1 nm. No mobility enhancement due to strain engineering is assumed.

Fig. 1 shows schematic illustrations of the FinFET structure. Design parameters are summarized in **Table I**. The fin width (W_{fin}) is 2/3 times L_G in order to suppress SCE, and the fin height (H_{fin}) is 4/3 times L_G in order to achieve layout efficiency comparable to planar MOSFET technology. For compact circuit layouts such as those used in SRAM cells, it is difficult to separately engineer the gate work functions (Φ_M) of the pull-down (PD) and pull-up (PU) devices because the gate layer fills the entire region in-between the n-channel and p-channel fins [11]. Therefore, a single near-midgap gate work function is assumed. The electrical channel length (L_{eff}) was selected to maximize drive current (I_{ON}) for an off-state leakage current (I_{OFF}) of 3 nA/μm, corresponding to the ITRS specification for low-operating-power applications [12].

Fig. 2 shows a cross-sectional schematic of the planar FD-SOI MOSFET structure. Design parameters were selected according to [13] for superior SCE control, and are summarized in **Table II**. Φ_M values were selected for I_{OFF} = 3 nA/μm.

SOI MOSFET Performance

Figs. 3a and 3b show simulated transfer (I_D-V_{GS}) curves for the nominal optimized n-channel and p-channel FinFET designs with Φ_M = 4.6 eV, respectively. Variation due to RDF and gate-LER was evaluated using 3D Kinetic Monte Carlo simulations, 100 cases (**Fig. 3c**). The gate LER profiles were obtained using 100 different gate-line profiles derived from a scanning electron microscopy image of photoresist lines processed for the 22 nm node. Note that the transistor current is normalized to the channel width, which is $2H_{fin}$ [14]. In practice, the circuit designer can adjust the effective channel width of a SOI FinFET (to adjust its drive strength) only in increments of $2H_{fin}$, by increasing/decreasing the number of fins in parallel. Thus, it is not possible to finely adjust the beta (β) ratio of a SOI FinFET-based SRAM cell.

Figs. 4a and 4b show simulated transfer curves for the nominal optimized n-channel and p-channel planar FD-SOI MOSFET designs, respectively. Note that the I_{ON} values are slightly lower, but that SCE suppression is superior, for these devices in comparison against the FinFETs. (Steeper sub-threshold swing, SS, and reduced drain-induced barrier lowering, DIBL, are seen in the planar FD-SOI devices *vs*. the FinFET devices.) Accordingly, less variation in V_{TH} due to RDF is seen for the planar FD-SOI MOSFET (**Fig. 4c**).

In this work, the standard deviation of variation in saturation threshold voltage due to gate work function variation (WFV) was estimated based on [15]. The random sources of variation

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(RDF, gate LER, and WFV) are assumed to be statistically independent. Their additive impacts on the standard deviation of saturation threshold voltage variation, $\sigma(V_{T,SAT})$, for FinFET and planar FD-SOI SRAM pull-down devices are indicated in **Table III**. Note that the planar FD-SOI structure has smaller $\sigma(V_{T,SAT})$ due to its superior electrostatic integrity.

6-T SRAM Cell Designs

A simple analytical model was fit to simulated I_D-V_{GS} and I_D-V_D characteristics for each SOI MOSFET design, to allow for fast estimation of SRAM metrics such as read static noise margin (RSNM) [16] and writeability current (I_w) [17].

The FinFET SRAM cell dimensions shown in **Fig. 5** were selected by linearly scaling the FinFET-based SRAM cell in [18]. The cell β ratio is either 1 if single-fin-PD devices are used or 2 if dual-fin-PD devices are used. As a result, there is a trade-off in cell area for improved read margin, unless a pitch-halving technique such as spacer lithography [19] is used.

The planar FD-SOI SRAM cell dimensions shown in **Fig. 6** were selected by following the 22 nm design rules in [20]. The planar FD-SOI cell (with β ratio = 1.375) is as compact as the single-fin-PD FinFET cell and offers a read margin that is comparable to that of the dual-fin-PD FinFET cell (**Table IV**). Due to higher I_{ON}, I_w is significantly higher for the FinFET cells than for the planar FD-SOI cell.

SRAM Yield Estimation

Cell sigma, defined as the minimum amount of variation for DC read/write failure [21], is used herein to assess SRAM yield. Random variations due to gate-LER, RDF and WFV, as well as process-induced variations (±10%) in L_G, T_{ox}, Si fin/channel width, and Si height/thickness are considered. **Fig. 7** shows that the SOI FinFET SRAM cells as designed cannot to meet the six-sigma yield requirement, in contrast to the planar FD-SOI SRAM cell. This is due to the larger sensitivities of the FinFET to random and process-induced variations, and is consistent with the findings in [6] and [18].

Fig. 8 shows the effect of fine-tuning Φ_M on SOI FinFET SRAM yield. Note that L_{eff} is optimized to maximize I_{ON} at each value of Φ_M (ref. Table IIIa). When Φ_M is increased slightly, NMOS $|V_{TH}|$ increases whereas PMOS $|V_{TH}|$ decreases; also, the optimal NMOS L_{eff} decreases whereas the optimal PMOS L_{eff} increases. The reduction in NMOS L_{eff} results in worse SCE and hence larger $\sigma(V_{T,SAT})$, so that RSNM yield is degraded. The reduction in PMOS $|V_{TH}|$ results in degraded writeability. Thus, it will be difficult for FinFET-based SRAM technology to meet the six-sigma yield requirement, unless narrower fin widths (less than 2/3 times L_G) are used to better suppress variation.

Conclusion

FinFETs can have superior performance (I_{ON}/I_{OFF}) but increased sensitivity to process-induced variations, as compared against thin-BOX planar FD-SOI MOSFETs. The fin width must be less than 2/3 times L_G in order for SOI FinFET technology to meet the six-sigma SRAM yield requirement at the 22 nm CMOS technology node. Thin-BOX planar FD-SOI MOSFET technology can meet this requirement with a body thickness that is ~1/4 times L_G.

References

[1] M.J.M. Pelgrom *et al*., *IEEE J. Solid-State Circuits*, p. 1433, 1989.
[2] K.J. Kuhn, *IEDM Tech. Dig*., 2007.
[3] A. Asenov, *Symp. VLSI Tech.*, 2007.
[4] D. Hisamoto *et al*., *IEEE Trans. Electron Devices*, p. 2320, 2000.
[5] N. Lindert *et al*., *IEEE Electron Device Lett*., p. 487, 2001.
[6] A.V.-Y. Thean *et al*., *IEDM Tech. Dig.*, 2006.
[7] A. Dixit *et al*., *IEDM Tech. Dig.,* 2006.
[8] T. Ohtou *et al.*, *IEEE Electron Device Lett*., p. 740, 2007.
[9] C. Fenouillet-Beranger *et al*., *Solid-State Electronics*, p. 730, 2009.
[10] Sentaurus User's Manual, v. 2009.06 (Synopsys, Inc.)
[11] V. Varadarajan and T.-J. King Liu, *UGIM Symposium*, 2006.
[12] *Int'l Tech. Roadmap for Semiconductors*, 2007 Ed.
[13] K. Cheng *et al*., *Symp. VLSI Tech.*, 2009.
[14] J.G. Fossum *et al*., *IEDM Tech. Dig.,* 2004.
[15] H. Dadgour *et al*., *IEDM Tech. Dig.*, 2008.
[16] E. Seevinck *et al., JSSC*, p. 748, 1987.
[17] C. Wann *et al., VLSI-TSA*, 2005.
[18] H. Kawasaki *et al*., *IEDM Tech. Dig.*, 2008.
[19] Y.-K. Choi *et al*., *IEEE Trans. Electron Devices*, p. 436, 2002.
[20] B.S. Haran *et al*., *IEDM Tech. Dig*., 2008.
[21] A. Carlson, *IEEE Si Nanoelectronics Workshop,* 2008.

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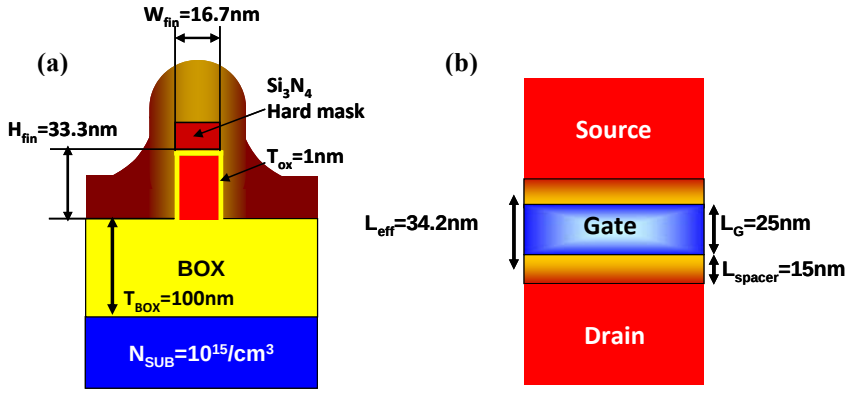


Fig. 1: Schematic illustrations of the SOI FinFET structure: **(a)** cross-sectional view, **(b)** plan view. Ohmic contacts are made to the source/drain top surfaces.

	NMOS	PMOS
L_G (nm)	25	25
L_{eff} (nm)	34.2	30.1
T_{ox} (nm)	1	1
W/L_G	2/3	2/3
H/L_G	4/3	4/3
Φ_M (eV)	4.6	4.6

Table I: SOI FinFET design parameters.

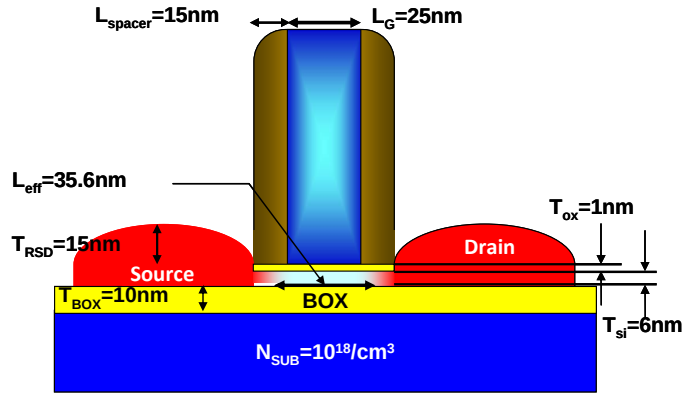


Fig. 2: Schematic cross-section of the FD-SOI MOSFET structure. Ohmic contacts are made to the source/drain top surfaces.

	NMOS	PMOS
L_G (nm)	25	25
L_{eff} (nm)	35.6	30.7
T_{ox} (nm)	1	1
T_{BOX} (nm)	10	10
T_{Si} (nm)	6	6
Φ_M (eV)	4.45	4.85

Table II: FD-SOI MOSFET design parameters.

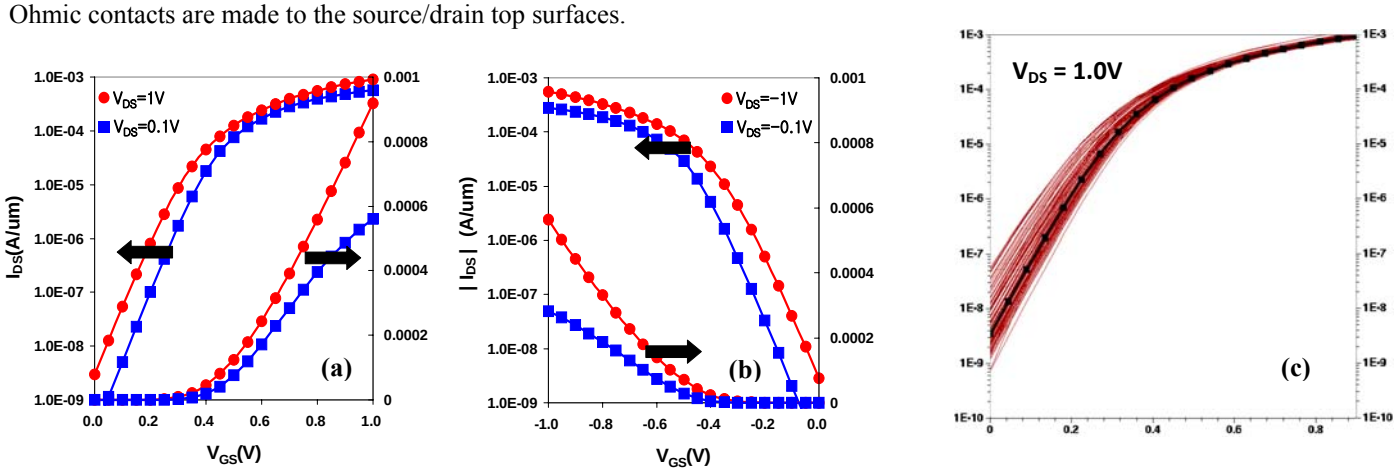


Fig. 3: Simulated SOI FinFET I_{DS}-V_{GS} curves: **(a)** nominal NMOS, **(b)** nominal PMOS, **(c)** NMOS with atomistic doping profiles and gate line edge roughness (100 cases shown; nominal case shown in black).

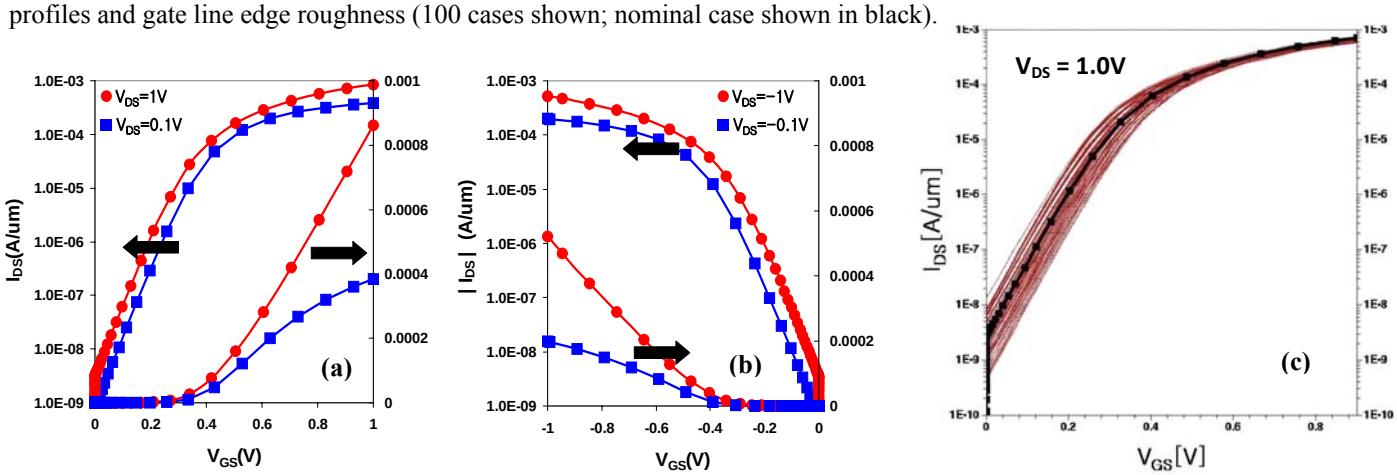


Fig. 4: Simulated FD-SOI MOSFET I_{DS}-V_{GS} curves: **(a)** nominal NMOS, **(b)** nominal PMOS, **(c)** NMOS with atomistic doping profiles and gate line edge roughness (100 cases shown; nominal case shown in black).

	Φ_M = 4.6eV		Φ_M = 4.65eV		Φ_M = 4.7eV	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
I_{ON} (μA/μm)	918	563	885	580	833	575
I_{OFF} (nA/μm)	3	3	3	3	3	3
$\|V_{T,LIN}\|$ (mV)	200	241	227	214	252	186
$\|V_{T,SAT}\|$ (mV)	123	135	129	128	136	120
DIBL (mV/V)	86	118	109	96	129	73
S.S. (mV/dec)	78	84	82	79	86	75
$\sigma V_{T,SAT}$ (mV)$\|_{LER}$	29	39	32.4	30.1	46	19.6
$\sigma V_{T,SAT}$ (mV)$\|_{LER+RDF}$	31.3	43.7	44.9	40.8	58.4	28.4
$\sigma V_{T,SAT}$ (mV)$\|_{LER+RDF+WFV}$	32.9	44.9	45.7	41.7	59.0	29.7

(a)

	NMOS	PMOS
I_{ON} (μA/μm)	861	518
I_{OFF} (nA/μm)	3	3
$\|V_{T,LIN}\|$ (mV)	160	182
$\|V_{T,SAT}\|$ (mV)	114	116
DIBL (mV/V)	51	73
S.S. (mV/dec)	75	78
$\sigma V_{T,SAT}$ (mV)$\|_{LER}$	10	14
$\sigma V_{T,SAT}$ (mV)$\|_{LER+RDF}$	22.3	26.1
$\sigma V_{T,SAT}$ (mV)$\|_{LER+RDF+WFV}$	25.5	28.9

(b)

Table III: Simulated transistor performance parameters for V_{DD}=1.0V: **(a)** SOI FinFET, **(b)** FD-SOI MOSFET.

	Single-fin FinFET	Dual-fin FinFET	FD-SOI
RSNM [mV]	142.3	190.5	186
I_w [uA]	33.0	28.4	18.9
Area [um^2]	0.075	0.079	0.075

Table IV: Comparison of SRAM read/write margins and cell areas, for V_{DD}=0.9V.

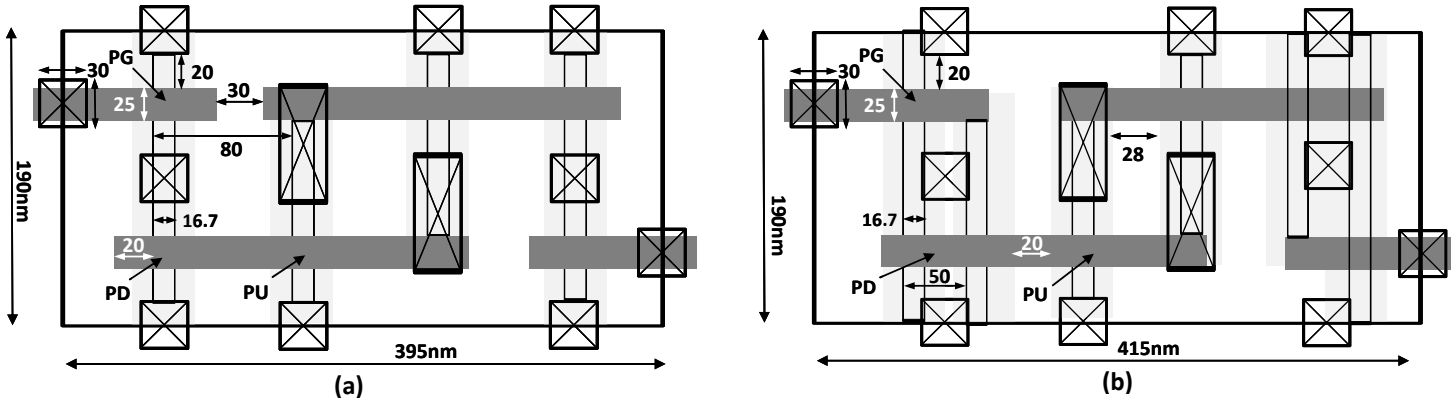
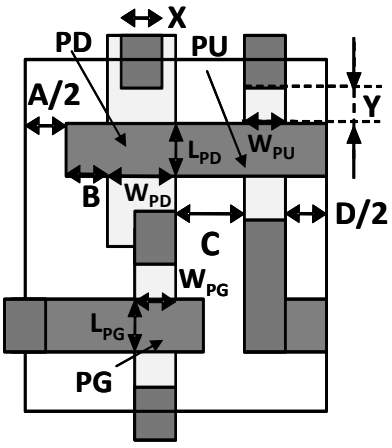


Fig. 5: SOI FinFET SRAM cell layouts: **(a)** single-fin pull-down devices (β ratio = 1), **(b)** dual-fin pull-down devices (β ratio = 2).



Design rules		Symbol	Size [nm]
Cell Height	PG CH length	L_{PG}	25
	PD CH length	L_{PD}	25
	CONT size	X	30
	Gate-to-CONT	Y	20
	Total	190	
Cell Width	POLY-to-POLY	A	30
	POLY-to-DIF ext	B	20
	PD Width	W_{PD}	55
	N/P isolation	C	50
	PU width	W_{PU}	32
	DIF-DIF (min)	D	50
	PG width	W_{PG}	40
	Total	394	
A SRAM cell area		0.07486 μm^2	

Fig. 6: FD-SOI SRAM half-cell layout **(left)** and dimensions **(right)**.

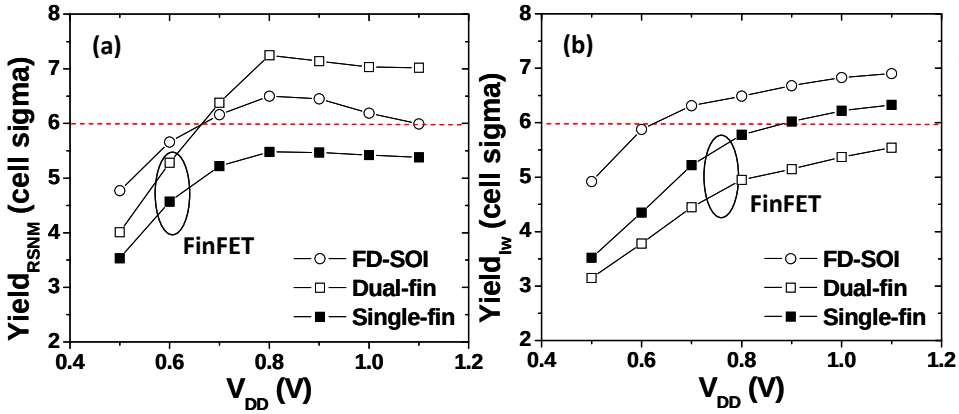


Fig. 7: Estimated SRAM cell yield for Φ_M=4.6eV, as a function of cell operating voltage: **(a)** yield of read static noise margin (RSNM), **(b)** yield of write-ability current (I_w).

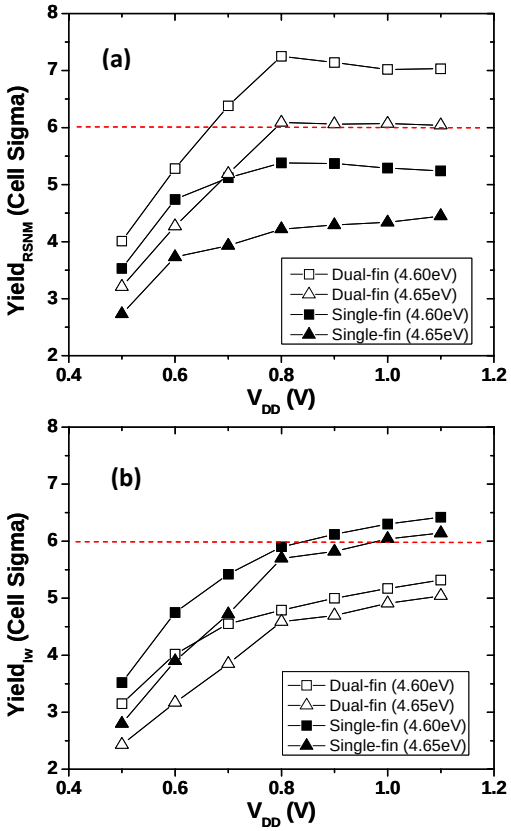


Fig. 8: Impact of gate work function on estimated FinFET SRAM cell yield. **(a)** yield of read static noise margin (RSNM), **(b)** yield of write-ability current (I_w).