Discrete-Time, Cyclostationary Phase-Locked Loop Model for Jitter Analysis

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Abstract – **Timing jitter is one of the most significant phase-locked loop characteristics, with high impact on performance in a range of applications. It is, therefore, important to develop the tools necessary to study and predict PLL jitter performance at design time. In this paper a discrete-time, linear, cyclostationary PLL model for jitter analysis is proposed, which accounts for the cyclostationary nature of noise injected into the loop at various PLL components. The model also predicts the aliasing of jitter due to the downsampling and upsampling of frequencies around the PLL loop. Closed-form expressions are derived for the output jitter spectrum and match well with results of event-driven simulations of a 3rd-order PLL.**

I. Introduction

Timing jitter is one of the most important performance metrics for the steady-state operation of a phase-locked loop (PLL) circuit. It contributes to synchronization problems and is a major source of bit errors in wireless and wireline communication systems. It is, therefore, crucial to develop the analytical tools necessary to correctly study and predict the jitter performance of the PLL output clock.

Jitter behavior in a PLL circuit can be studied through the use of stochastic differential equations [1]. This approach, although mathematically elegant, may be too complex for use in practical designs. A more conventional approach for studying PLL jitter is by assuming a continuous-time, linear, time-invariant model for the PLL circuit [2]. Even though this approximation yields useful results under certain conditions, it fails to capture two important features of PLL noise, the cyclostationary noise injection and aliasing. This paper presents an extension of PLL jitter theory, which accounts for the effects of aliasing in the PLL loop and also provides a general approach to incorporate the cyclostationary nature of PLL noise sources in the jitter analysis.

The cyclostationary mechanism converts the supply/substrate and device noise of PLL components like voltage-controlled oscillator (VCO), charge pump and VCO output buffer into noise injected into the PLL loop. The mechanism, which translates the supply/substrate or device noise into phase noise at the output of a standalone VCO, has been examined in the literature [3]. However, limited attempts have been made to develop a PLL model that deals with the cyclostationary nature of the noise injected into the PLL loop [4]. Using the circuit-independent description of cyclostationary phase noise introduced in [3], in this paper we present a more general study of the effects of cyclostationarity on PLL jitter.

Noise aliasing is a second issue that is not captured with the customary continuous-time, linear, time-invariant PLL model. When the frequency multiplication factor N in a PLL is different than unity, the divide-by-N circuit essentially acts as a downsampling block. If PLL jitter is modeled as a discrete-time signal at clock edges, it is downsampled and upsampled as it propagates around the PLL loop, and may get aliased. To capture this effect, a discrete-time model for the PLL is needed. The existing discrete-time PLL models do not capture this effect, since they either consider only PLLs with a frequency multiplication factor N equal to one [5],[6] or model the divide-by-N circuit simply as a $1/N$ phase divider [7].

The next section develops the discrete-time, linear, cyclostationary jitter model for the 3rd-order PLL. This is accomplished in three stages: First, the discrete-time equations, which describe the individual PLL components, are presented in Section II.A. Then, the cyclostationary mechanism, which converts supply or device noise to loop-injected noise, is described for the VCO and other components, and the spectral characteristics of the resulting noise sources are derived in Section II.B. To complete the model, the transfer functions from the various noise nodes to the output jitter are calculated for the discrete-time PLL model in Section II.C. Finally, in Section III, the theoretical results are verified using behavioral simulations of 3rd-order PLL circuits in various noise scenarios.

II. Discrete-Time, Cyclostationary PLL Model

This section develops the discrete-time, linear, cyclostationary model for a 3rd-order PLL. Fig. 1 shows the discrete-time model of the 3rd-order PLL used in the subsequent analysis. The divide-by-N component is modeled as a downsampling-by-N block.

The upsampling block introduces N-1 zeros between successive pulses of charge pump current. This corresponds to the physical reality that the charge pump is activated only once every N PLL clock cycles, in order to adjust the VCO control voltage, while it remains off during the rest of the time.

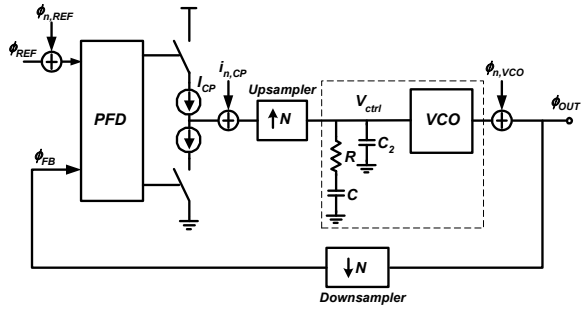

Fig. 1: Discrete-time model of 3rd-order PLL with noise sources.

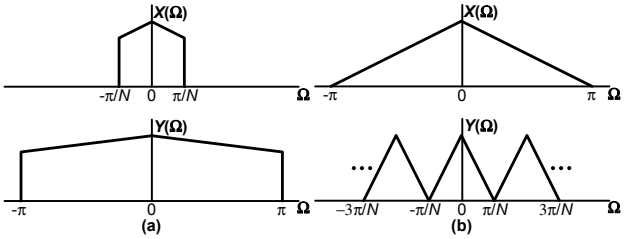

Fig. 2: Signal spectra in a) downsampling-by-N and b) upsampling-by-N blocks.

A. Discrete-Time Equations for PLL Components

This subsection derives the discrete-time transfer functions for the various PLL components in Fig. 1. It should be noted that the Fourier transforms shown in the following are periodic functions with period equal to 2π.

The output spectrum $Y(\Omega)$ of the downsampling-by-N block is related to its input spectrum $X(\Omega)$ through the following equation [8]:

$$Y(\Omega)=\frac{1}{N}\cdot\sum_{k=0}^{N-1}X\left(\frac{\Omega-2\pi k}{N}\right) \tag{1}$$

The output spectrum of the upsampling-by-N block is related to its input spectrum as follows [8]:

$$Y(\Omega)=X(\Omega\cdot N) \tag{2}$$

Fig. 2 graphically depicts the relationship between the input and output spectra for the downsampling and upsampling blocks.

The conversion gain of the combination of the phase-frequency detector (PFD) and the charge pump is given by:

$$K_p=\frac{I_{CP}}{f_{PLL}} \tag{3}$$

The discrete-time transfer function of the combination of the loop filter and VCO is obtained through the impulse-invariant transformation technique [5] and can be shown to be equal to [9]:

$$H_{LF,VCO}(\Omega)=\frac{A}{\left(1-e^{-j\Omega}\right)^2}+\frac{B}{1-e^{-j\Omega}}+\frac{E}{1-e^{-\frac{C+C_2}{CC_2R}T}\cdot e^{-j\Omega}} \tag{4}$$

where the coefficients are given by the following equations:

$$A=\frac{K_V\cdot T}{C+C_2},\ B=\frac{K_V C^2R}{(C+C_2)^2}\ \text{and}\ E=-\frac{K_V C^2R}{(C+C_2)^2}.$$

In the above expressions, K_V is the frequency gain of the VCO and T is the period of the PLL output clock.

B. Cyclostationary Behavior of PLL Noise Sources

The cyclostationary mapping of supply and/or device noise from various PLL components into noise injected in the PLL loop can be described by the "Impulse Sensitivity Function" (ISF) [3].

Fig. 3 explains this concept in the case of device noise injected into a standalone VCO. Assuming that the injected noise is a current impulse, it will produce a step response in the VCO phase, because the momentary phase disturbance produced by the current impulse circulates around the VCO stages ad infinitum. The magnitude of this step response is dependent on the time instant within a VCO oscillation period, at which the current impulse is applied. A similar response is produced by a voltage impulse on the VCO supply.

The phase impulse response of a standalone VCO to either supply or device noise is given by the following expression:

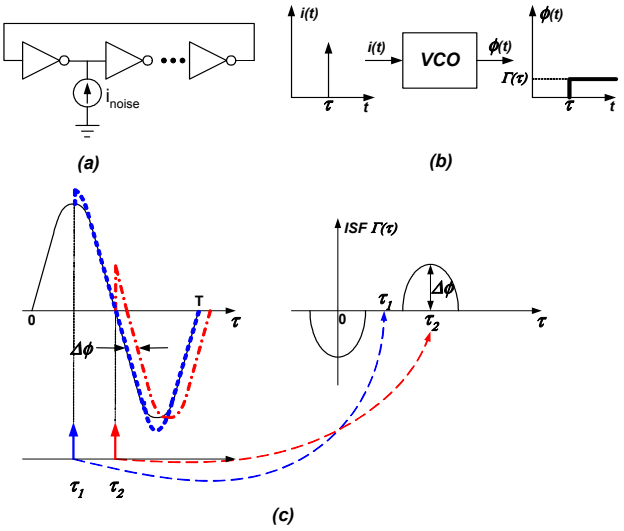

Fig. 3: ISF mechanism for VCO device noise: (a) Current impulse injected into a VCO node, (b) Phase step response of the VCO to the injected current impulse, (c) Current impulses injected at different time instants produce different phase step magnitudes.

$$h_{\varphi_{n,VCO}}(t,\tau)=\Gamma_{p,VCO}(\tau)\cdot u(t-\tau) \tag{5}$$

where τ is the time instant, at which the noise impulse is applied, $u(t)$ is the step function, and $\Gamma_{p,VCO}(\tau)$ is a periodic function with period equal to that of the VCO oscillation, and whose value at τ is the magnitude of the phase step produced by the noise impulse. The function $\Gamma_{p,VCO}(\tau)$ is the ISF of the VCO and can be written as:

$$\Gamma_{p,VCO}(\tau)=\sum_{n=-\infty}^{\infty}\Gamma_{VCO}(\tau-nT) \tag{6}$$

where $\Gamma_{VCO}(\tau)$ denotes one period of the ISF. The phase response of the VCO to an arbitrary noise disturbance is given by the following superposition integral (taking into account the periodicity of the ISF):

$$\begin{aligned}\varphi_{n,VCO}[k]\equiv\varphi_{n,VCO}(kT)&=\int_{-\infty}^{kT}\Gamma_{p,VCO}(\tau)\cdot i(\tau)d\tau\\&=\varphi_{n,VCO}[k-1]+\int_{0}^{T}\Gamma_{VCO}(\tau)\cdot i(\tau+(k-1)T)d\tau\end{aligned} \tag{7}$$

where $i(\tau)$ denotes the supply or device noise waveform. Fig. 4 shows one period of the ISFs that correspond to supply and device noise of a VCO designed in 0.13 μm CMOS. The ISFs were extracted using transistor-level simulations for a VCO comprised of 4 differential stages and operating at 2 GHz by measuring the magnitudes of the phase steps when applying impulses on the VCO supply or internal nodes at different instances during the VCO period.

A similar approach using the generalized ISF concept can give the current noise at the output of the charge pump or the phase noise at the output of the VCO buffer [9]. The main difference with the VCO case is that the noise accumulates over a finite period of time.

Using the above equations, it is possible to derive the spectrum of the noise injected into the PLL loop for some

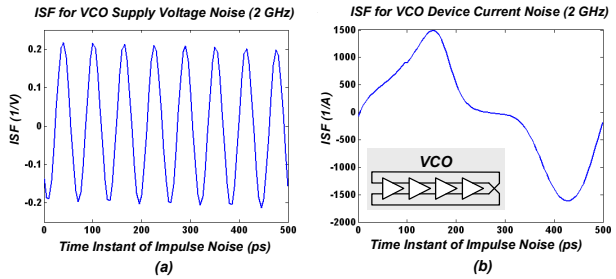

Fig. 4: VCO impulse sensitivity functions: (a) Supply noise, (b) Device noise in one VCO node. The VCO is comprised of four differential stages.

important types of supply or device noise, such as impulse, sinusoidal or white [9].

a) Let the supply or device noise $i(\tau)$ be a deterministic impulse function given by $i(\tau)=A\cdot\delta(\tau-\tau'_0)$ where $\tau'_0=(k_0-1)T+\tau_0$ with $0\le\tau_0<T$ and k_0 integer. Then, from (7), the output phase is $\phi_{n,VCO}[k]=A\cdot\Gamma_{VCO}(\tau_0)\cdot u[k-k_0]$ where $u[\cdot]$ the step function. Hence, the discrete-time Fourier transform (DTFT) of the injected phase noise to the PLL loop at the output of the VCO is:

$$\Phi_{n,VCO}(\Omega)=A\cdot\Gamma_{VCO}(\tau_0)\cdot\frac{e^{-j\Omega k_0}}{1-e^{-j\Omega}} \tag{8}$$

b) Let the supply or device noise $i(\tau)$ be a deterministic sinusoidal function given by $i(\tau)=A_1\cdot cos(\omega'_1 t+\theta_1)$. From equation (7) we have:

$$\Phi_{n,VCO}(\Omega)=\Phi_{n,VCO}(\Omega)\cdot e^{-j\Omega}+\int_0^T\Gamma_{VCO}(\tau)\cdot\left[\sum_{k=-\infty}^{\infty}e^{-j\Omega k}\cdot i(\tau+(k-1)T)\right]d\tau \tag{9}$$

The quantity in brackets is the DTFT of the sequence $i[k]\equiv i(\tau+(k-1)T)$. This can be calculated and used in (9) to get the DTFT of the VCO noise injected into the loop:

$$\Phi_{n,VCO}(\Omega)=\frac{\pi}{1-e^{-j\Omega}}\cdot\{Q_1(\omega'_1,\theta_1)\cdot\delta(\Omega-\omega_1T)+Q_2(\omega'_1,\theta_1)\cdot\delta(\Omega+\omega_1T)\} \tag{10}$$

where

$$Q_1(\omega'_1,\theta_1)=\int_0^T\Gamma(\tau)\cdot[Q_c(\tau,\omega'_1,\theta_1)-jQ_s(\tau,\omega'_1,\theta_1)]d\tau$$

$$Q_2(\omega'_1,\theta_1)=\int_0^T\Gamma(\tau)\cdot[Q_c(\tau,\omega'_1,\theta_1)+jQ_s(\tau,\omega'_1,\theta_1)]d\tau$$

with

$$Q_c(\tau,\omega'_1,\theta_1)=A_1\cdot cos[\omega'_1\cdot\tau-\omega'_1\cdot T+\theta_1]$$
$$Q_s(\tau,\omega'_1,\theta_1)=A_1\cdot sin[\omega'_1\cdot\tau-\omega'_1\cdot T+\theta_1]$$

Also $\omega_1T=\omega'_1T\ \ mod\ \ 2\pi$.

A similar approach gives the noise spectrum injected at the VCO output when $i(\tau)$ is white. Also, similar analysis can be used to derive the noise spectra at the charge pump and VCO buffer outputs for impulsive, sinusoidal and white supply or device noise. The details of the analysis are presented in [9].

C. Closed Loop Noise Transfer Functions

In order to complete the PLL jitter model, it is necessary to calculate the closed-loop transfer functions from the various noise sources to the PLL output. In the case when the noise source is the reference clock jitter, then the spectrum of the PLL output jitter is given by the following expression [9]:

$$Y_{REF}(\Omega)=\frac{H(\Omega)}{1+\frac{1}{N}\sum_{k=0}^{N-1}H\left(\Omega-\frac{2\pi k}{N}\right)}\cdot X_{REF}(N\cdot\Omega) \tag{11}$$

where $H(\Omega)=K_P\cdot H_{LF,VCO}(\Omega)$ with K_P, $H_{LF,VCO}(\Omega)$ as defined in section II.A. The quantity $X_{REF}(\Omega)$ is the reference clock jitter spectrum. The above equation indicates that spectral images will be present at the output jitter spectrum due to upsampling of the input noise, as shown by the term $X_{REF}(N\cdot\Omega)$.

In the case of VCO noise, the output jitter is given by the following expression [9]:

$$Y_{VCO}(\Omega)=X_{VCO}(\Omega)-\frac{1}{N}\frac{\sum_{k=0}^{N-1}X_{VCO}\left(\Omega-\frac{2\pi k}{N}\right)}{1+\frac{1}{N}\sum_{k=0}^{N-1}H\left(\Omega-\frac{2\pi k}{N}\right)}\times H(\Omega) \tag{12}$$

where $H(\Omega)$ as defined above and $X_{VCO}(\Omega)$ the VCO noise spectrum. In this case the jitter aliasing is apparent due to the $\sum_{k=0}^{N-1}X_{VCO}\left(\Omega-\frac{2\pi k}{N}\right)$ term. Similar analysis can give the discrete-time PLL loop dynamics when the noise is injected at the charge pump or VCO output buffer [9]. Since the PLL model is linear, superposition applies when more than one noise types are present.

III. Simulation Results

This section presents results from event-driven simulations using Verilog-A by Cadence [10], which are compared to the theoretical expressions derived in the previous section. The phase of the VCO is computed as the sum of two terms. The first is the integral of the simulation time and corresponds to the case of a noiseless VCO. The second term is the integral of the VCO noise waveform weighted by the ISF. When the total phase reaches multiples of π, a transition of the VCO voltage waveform occurs. In the following, the VCO ISF is modeled as a sinusoidal function with a small DC component after the extracted ISF of Fig. 4(a).

In order to verify the PLL model developed in the previous sections, we first apply impulse noise on the VCO supply at two different time instances as shown in Fig. 5. The simulation plot is obtained from the FFT of the impulse response, while the theoretical plot is calculated from (12) with $X_{VCO}(\Omega)$ given in (8). Fig. 5 shows the spectra of the PLL output jitter in the two cases when a VCO supply noise impulse is applied at the maximum and 40% of the maximum of the VCO ISF. Comparing the plots of Fig. 5(a) and Fig. 5(b) shows a change in the magnitude of the jitter spectrum as a result of the cyclostationary nature of the VCO noise. Such a behavior cannot be predicted by a time-invariant PLL jitter model, yet is critical to capture in digital applications where most of the noise events are synchronized to a clock and are not time-invariant.

In order to study the aliasing effects of jitter, sinusoidal voltage noise at 190 MHz is applied on the VCO supply at a PLL operating frequency of f_{PLL}=1 GHz and divide ratio N=5. The loop bandwidth of the PLL is 10 MHz. Fig. 6 shows the PLL output jitter spectrum normalized to the amplitude of the input noise. The theoretical plot is obtained by using (10) for the input noise spectrum and (12) for the PLL loop behavior. The various spurs that appear in the spectrum can be justified as follows: The PLL jitter spectrum is periodic with a period equal to 1 GHz and it is

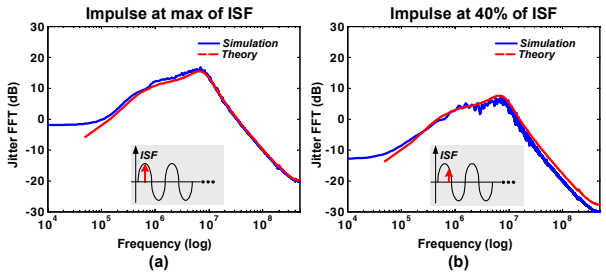

Fig. 5: Normalized spectrum of PLL output jitter when applying a VCO supply noise impulse. The PLL operating frequency is 1 GHz and the divide ratio is N=5. The VCO supply noise impulse is applied (a) at the ISF maximum, (b) at 40% of the ISF maximum.

also symmetric around DC. Therefore, the spectrum is fully characterized by its content in the frequency range from DC to 500 MHz as shown in Fig. 6. From (12) it can be seen that there are N-1=4 spurs that are predicted by the theory in addition to the spur at the input noise frequency of f_0=190 MHz. From (12) and taking again the periodicity and symmetry of the spectrum into account, these spurs appear at the following frequencies:

$$f_k = f_0 + k \times \frac{f_{PLL}}{N} = 390,\ 410,\ 210,\ 10 \text{ MHz for } k=1,\ldots,4.$$

These frequencies are denoted in Fig. 6. It should be noted here that the jitter spectrum in Fig. 6(a), which is obtained through simulation, exhibits a harmonic spur at $2 \cdot f_0$=380 MHz. This harmonic is due to nonlinearities in the simulation process and cannot be predicted by the PLL model, since it is linear. The agreement in the magnitudes of the main spurs (10 MHz and 190 MHz) between simulation and theory is within 1%. The agreement in the magnitudes of the secondary spurs is within 15%. Fig. 6 shows that even when the VCO supply noise frequency is out-of-band (as is the case with wideband supply noise), one of the resulting frequencies can fall in-band, thus potentially affecting the system performance. This effect cannot be predicted by a continuous-time model.

Fig. 7 shows the PLL output jitter spectrum when sinusoidal jitter of frequency 190 MHz is applied on the PLL reference clock. The PLL clock frequency is 1 GHz and the divide ratio is N=5, so that the reference clock frequency is f_{REF}=200 MHz. The reference clock jitter at 190 MHz is sampled at the reference clock frequency of 200 MHz and therefore it is aliased back to a spur at f_0=10 MHz. According to (11), the reference clock spectrum is upsampled by a factor of N=5, in order to produce the PLL output spectrum.

Therefore, the following spurs appear in addition to f_0, as predicted by (11) and shown in Fig. 7:

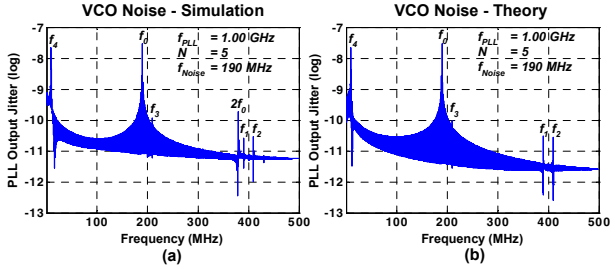

Fig. 6: Normalized output jitter spectrum due to VCO sinusoidal supply noise at 190 MHz. The PLL operating frequency is 1 GHz, the divide ratio N=5 and the loop bandwidth is 10 MHz. (a) Simulation, (b) Theory.

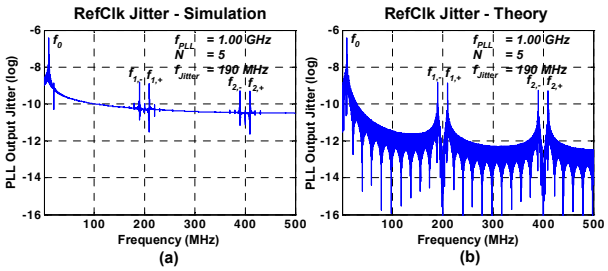

Fig. 7: Normalized output jitter spectrum due to reference clock sinusoidal jitter at 190 MHz. The PLL operating frequency is 1 GHz, the divide ratio N=5 and the loop bandwidth is 10 MHz. (a) Simulation, (b) Theory.

$$f_{k,\mp} = k \cdot f_{REF} \mp f_0 = 190,\ 210,\ 390,\ 410 \text{ MHz for } k=1,2.$$

IV. Conclusion

An extended discrete-time, linear, cyclostationary PLL model for jitter analysis is proposed. It accounts for the cyclostationary nature of noise injected into the PLL loop due to supply or device noise at the various components, and also captures the aliasing of jitter due to downsampling and upsampling of frequencies around the PLL loop, when the divide ratio N is greater than unity. Expressions were derived for the noise spectra injected into the loop by generalizing the mapping concept of Impulse Sensitivity Function. Capturing these cyclostationary and aliasing effects is critical in highly integrated digital applications where most noise sources (supply, substrate) are time-variant with spurious frequency content. Behavioral simulations of a 3rd-order PLL verify the theoretical results in the cases of VCO supply noise and reference clock jitter.

References

[1] A. Demir, "Computing timing jitter from phase noise spectra for oscillators and phase-locked loops with white and 1/f noise," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 53, no. 9, pp. 1869-1884, Sept. 2006.

[2] J. G. Maneatis, "Design of high-speed CMOS PLLs and DLLs," in *Design of High-Performance Microprocessor Circuits*, A. Chandrakasan et al., Ed., New York: IEEE Press, 2001, pp. 235-260.

[3] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, pp. 179-194, Feb. 1998.

[4] P. Heydari, "Analysis of the PLL jitter due to power/ground and substrate noise," *IEEE Trans. Circuits Syst. I: Regular Papers.*, vol. 51, pp. 2404-2416, Dec. 2004.

[5] J. P. Hein and J. W. Scott, "Z-Domain Model for Discrete-Time PLL's," *IEEE Trans. Circuits Syst.*, vol. 35, pp. 1393-1400, Nov. 1988.

[6] P. K. Hanumolu, M. Brownlee, K. Mayaram and U. K. Moon, "Analysis of Charge-Pump Phase-Locked Loops," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol 51, pp. 1665-1674, Sept. 2004.

[7] J. Lu, B. Grung, S. Anderson and S. Rokhsaz, "Discrete Z-Domain Analysis of High Order Phase Locked Loops," *Proceedings of the 2001 IEEE International Symposium on Circuits and Systems (ISCAS'01)*, vol. I, pp. 260-263.

[8] J. G. Proakis and D. G. Manolakis, *Digital Signal Processing: Principles, Algorithms and Applications*, 2nd Ed., New York: MacMillan, 1992.

[9] S. D. Vamvakos, "Analysis, Measurement and Optimization of Jitter in Phase-Locked Loops," *Ph.D. Dissertation*, Univ. of California, Berkeley, Dec. 2005.

[10] Cadence Design Systems, Inc., *Affirma™ Verilog-A Language Reference*, May 2001.