Fixed- and Variable-Length Ring Oscillators for Variability Characterization in 45nm CMOS

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***Abstract*- Fixed- and variable-length ring oscillators (RO's) are designed for characterization of circuit-topology induced variations and spatial correlations. A 930µm × 775µm test array is implemented in a low-power 45nm CMOS process. Measurements from the fixed-length RO's quantify an increase in variability with transistor stack height in logic gates and added variability associated to the top transistor in the stack. In addition, Variable-length RO's (VRO's) are designed to measure spatial correlation with a single-gate resolution.**

I. INTRODUCTION

With continued technology scaling, the increasing process variation remains a major roadblock in implementing high-performance digital circuits. Various ways of dealing with this problem have been suggested in different levels of abstraction from the architectural [1], the algorithmic [2], down to the circuit [3,4,5] level. On the other hand, the variability has been attributed to intrinsic device and interconnect performance, and layout variations. It has also been attributed in the past to circuit styles [6], but has not been studied in detail. In this work, we systematically characterize the impact of circuit topology on gate delay variability by measuring ring oscillator frequencies. Circuit topology delay dependence has a large impact on critical path monitoring used in adaptive throughput digital systems. Also, spatial correlation of variability greatly affects the use of statistical timing analysis. Although various measurement of the spatial correlation have been reported [7,8], the resolution of the measurements has been either too coarse or too fine to be useful in designing circuits. In this work, a VRO is designed to measure the correlation with a gate-level resolution.

II. TEST STRUCTURE

A 930µm × 775µm test array was built in a low-power 45nm CMOS process, consisting of 184 tiles of ROs and VROs. The VROs have three blocks of different implementations to measure the spatial correlation in different directions and gate orientations: 176 tiles of horizontal VROs, 210 tiles of vertical VROs, and 180 tiles of 90° (gate) rotated horizontal VROs (Fig.1). Dummy cells are added along the perimeter of each block to eliminate edge effects from the measurements.

A. RO structures

A tile of ROs is an aggregation of twenty ROs with inverting gates of different configurations. Fig.2 shows the gates devised to evaluate the effects of transistor stacking and switching order. The gates in the figure are grouped by the number of stacked PMOS and NMOS. Moreover, the top switching configuration is shown in the first column of the table. The number within a small box in the figure designates the index of the inverter. In addition, there are configurations for investigating the effect of pass transistors, layout symmetries, and layout rotation (Fig.3).

Each RO is composed of thirteen stages of inverting gates, accompanied with control logic to select and enable a single RO (Fig.5). The stage number of thirteen was chosen to keep the delay contribution of the enabling NAND gate less than 10% of the total delay. The output of the oscillator is multiplexed out to a frequency divider and the divided frequency is measured off-chip [7].

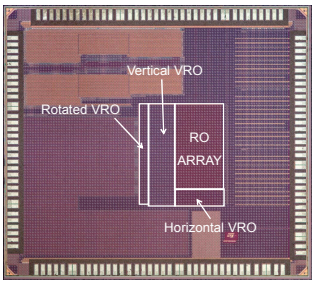


Fig.1: Chip microphotograph.

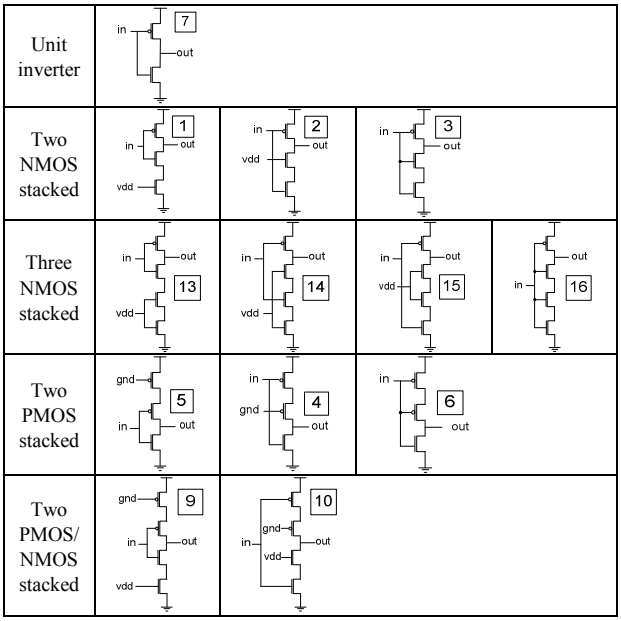
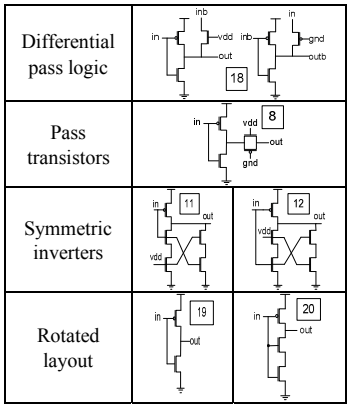


Fig.2: Test inverters for the effects of transistor stacking and switching order.



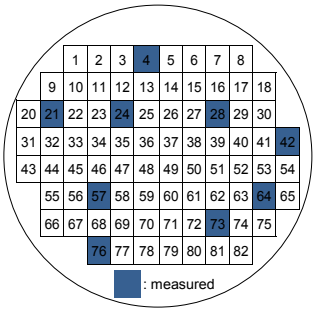


Fig.3: Test inverters for different logic. **Fig.4:** Dies measured within a wafer.

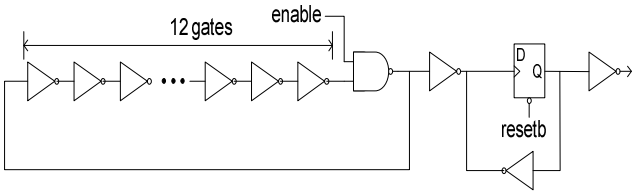


Fig.5: Ring oscillator diagram.

Frequencies of the ring oscillators from seventeen dies, from two positions in the reticle (A and B), scattered across a wafer were measured (Fig.4).

B. VRO structure

The VRO is devised to measure the spatial correlation with a gate-level resolution. A VRO tile has 26 selectable ring oscillator loops, each of which has different number of stages (Fig.6,8). The length of adjacent loops differs by four unit cells. The unit cell is made to have symmetric input loading (Fig.7) in order to maintain the same delay from either input signals. The horizontal VRO has the NAND gates placed horizontally adjacent to each other whereas the vertical VRO has the same gates placed vertically next to each other. The rotated VRO is a 90° rotated version of the horizontal VRO. In this case, the gates are rotated by 90°.

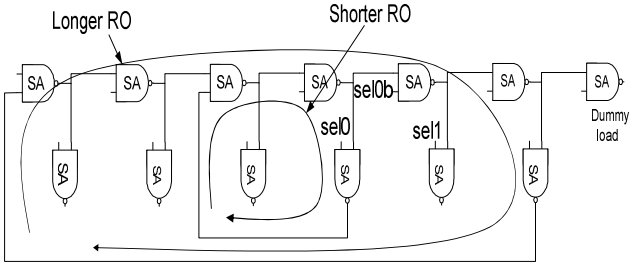


Fig.6: VRO diagram.

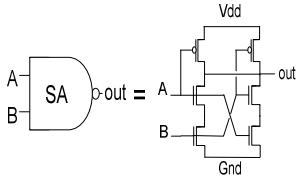


Fig.7: VRO unit cell.

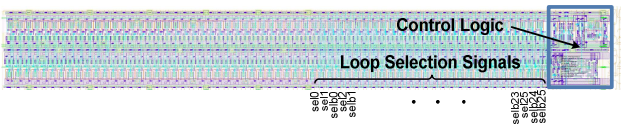


Fig.8: Horizontal VRO tile layout.

III. Measurement Results

The oscillating frequency of each RO was measured for more than one hundred cycles and an average value was taken as the frequency of the RO. The mean (μ) and the standard deviation (σ) of the frequencies are calculated over 184 ROs for an identical topology over the wafer.

A. RO Frequency Variation

Fig.9 shows the normalized σ of the measured frequencies plotted vs. the normalized mean frequency for the different inverter configurations in two dies of corner cases. The plot shows a strong correlation between the mean frequency and the variability of the circuit elements. Also, fig.10 is a plot of the normalized σ of three top switching configurations across all seventeen dies measured.

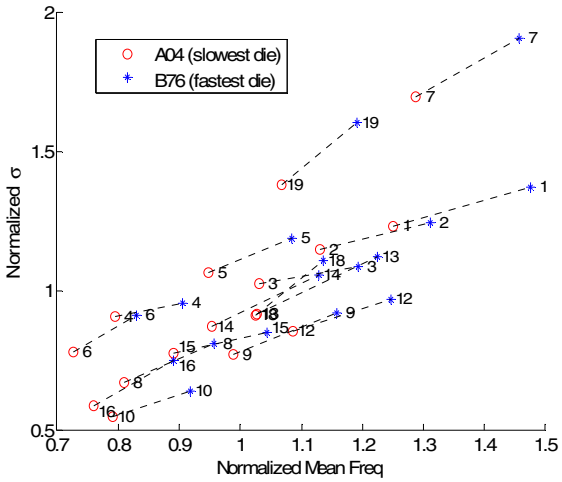


Fig.9: Measured σ vs. mean oscillating frequency. A number next to each point indicates the inverter index from Figs.2 and 3.

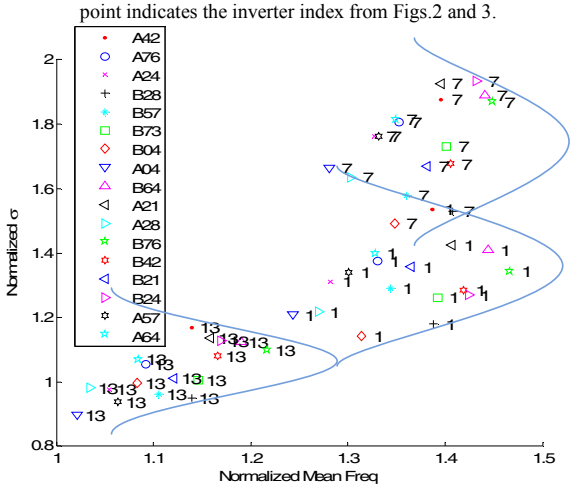


Fig.10: Measured σ vs. mean oscillating frequency over the wafer.

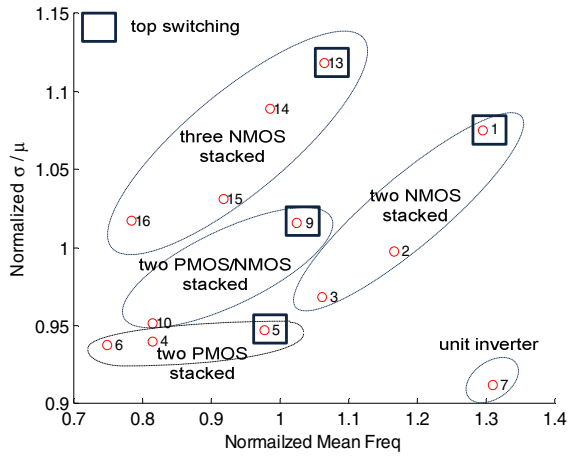


Fig.11: σ/μ plot of structures from Fig.2.

B. Transistor Stacking and Switching Order Effects

Fig. 11 is a plot of the measured σ/μ of the test structures described in Fig. 2 averaged over the wafer. From the plot, it can be observed that the taller the NMOS stack, the larger the variation. Also, the top switching configurations enclosed in boxes clearly show larger variability, which contributes to about 10% difference in σ/μ for the NMOS case and 3% difference for the PMOS. The PMOS top switching effect is not as pronounced as the NMOS one because of the larger speed gain associated with top switching in PMOS, which is due to the relatively larger internal capacitance of the PMOS stack structure. The increased variability of the top switching configuration can be qualitatively explained by the Id/Vds trajectory of the stacked configuration plotted in Fig.12. The trajectory of Id/Vds of a device during the switching is superimposed upon the Id/Vds characteristic curves of the device in the figure. It can observed that the top switching device clearly remains in the velocity-saturated (low-Vgs, high-Vds) region for a longer portion of its switching time. Because drive current, in this region of operation, has a stronger dependence on Vt, the performance of the top switching stack is more susceptible to process-induced variation in L and Vt.

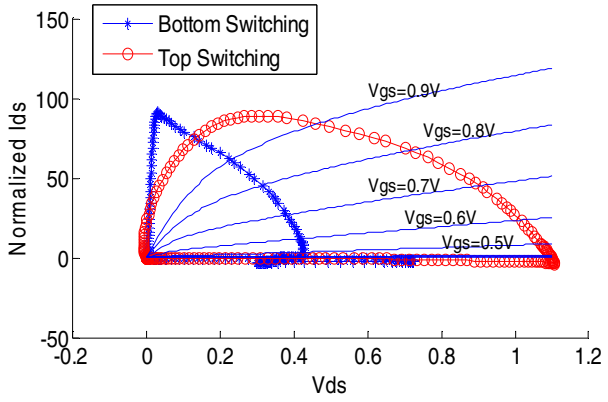


Fig.12: Id/Vds trajectories for top and bottom switching of two stacked NMOS's.

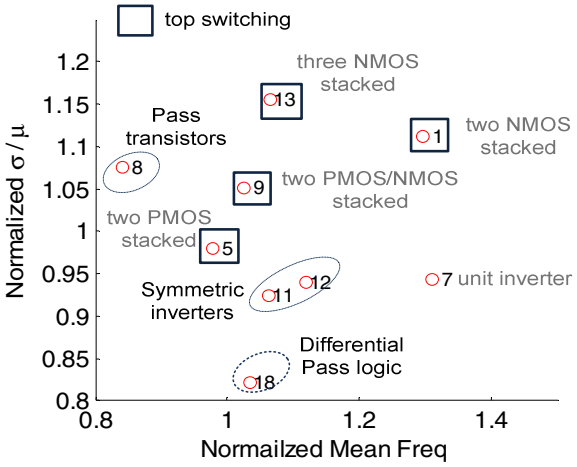


Fig.13: σ/μ plot for different styles.

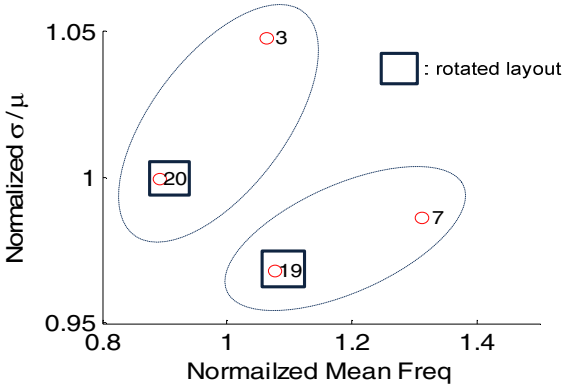


Fig.14: σ/μ plot for layout rotation.

C. Effects of Logic Styles and Layout Rotation

Fig.13 is a σ/μ plot for the test structures listed in Fig.3 that represent different logic styles. The differential pass logic has the least variability among all the structures examined, because it has the largest number of devices and the largest output capacitance, which both reduce sensitivity to variability. The relatively low variations of the symmetric inverters can also be explained in a similar way. In addition, as shown in Fig.14, only a minor difference in variability due to the direction of the layout (poly) is observed; inverters with horizontally drawn poly gates show slightly less variability (only 5% different in σ/μ) than normal poly gates largely because of lithography.

D. Spatial Correlation

Fig.15 shows the measured frequency distribution of VROs from a die. Different oscillating frequencies of individual loops within a VRO tile are clearly discernable. By denoting the oscillating frequency of the i^{th} loop of the j^{th} VRO cell as $f_{i,j}$, the delay of a unit cell between the i^{th} loop and the $(i+1)^{th}$ loop can be simply expressed as,

$$t_{i,j} = f_{i+1,j}^{-1} - f_{i,j}^{-1}.$$

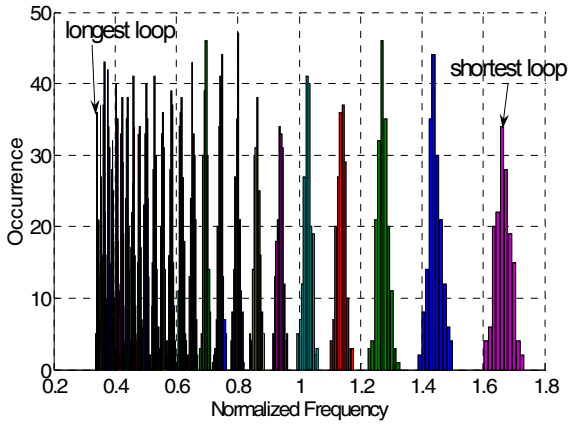


Fig.15: Oscillating frequency distribution of a horizontal VRO tile.

Fig.16 is a plot of this unit delay measured from a VRO tile. From this data, the covariance of the unit cell delays separated by τ unit cells can be calculated as,

$$C_j(\tau) = \mathbf{E}_i[(t_{i+\tau,j} - \mathbf{E}_j[t_{i+\tau,j}]) \cdot (t_{i,j} - \mathbf{E}_j[t_{i,j}])],$$

where $\mathbf{E}_j[\cdot]$ is an expectation operator over j. The spatial correlation can be calculated by the following equation,

$$R(\tau) = \mathbf{E}_j[C_j(\tau)] \Big/ \mathbf{E}_j[C_j(0)].$$

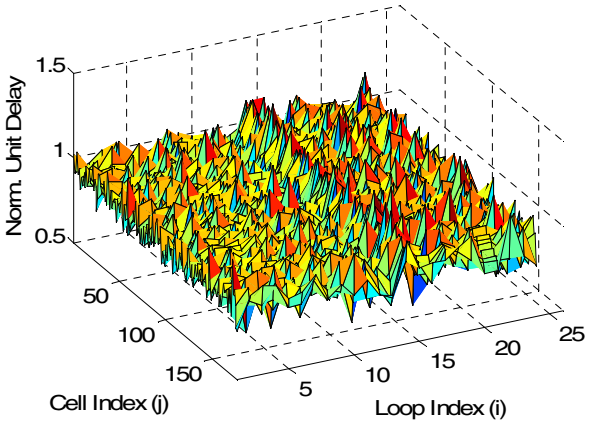


Fig.16: Unit delay of a horizontal VRO tile.

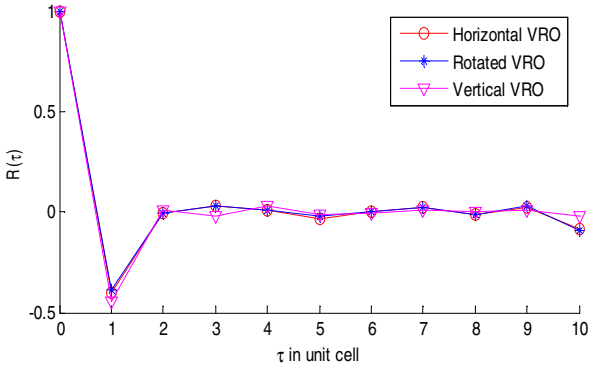


Fig.17: Spatial correlation of three types of the VRO structures.

Fig. 17 shows the spatial correlation calculated from the measurements and these equations. Except for the negative correlation with the nearest neighbor, attributed to the periodicity in wiring, the spatial correlation is weak for all three configurations of the VROs.

IV. Conclusion

Fixed- and variable-length ring oscillators are designed to evaluate the variability of different circuit topologies and spatial correlation of the variability, respectively, in a low-power 45nm CMOS process.

From the measurement results, it has been observed that the top switching configuration increases the random variation by 10% in the NMOS stack and 3% in the PMOS, compared to the switching of the bottom transistor. This finding has an impact on the design and design margins for circuits used for critical path monitoring in adaptive systems. While it has been measured that NMOS stacking increases the variability, the variation difference from the direction of the poly gate is observed as less than 5%. Also, from the VROs, weak spatial correlation in a gate-level resolution is measured.

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