High-CURRENT SnAPPACK Characteristics of MOSFET's

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Abstract—The high-current snappack characteristics of MOSFET's with different channel lengths and widths, gate oxide thicknesses, and substrate dopings were studied to determine their effectiveness in electrostatic discharge stress protection. Filamentary conduction was not observed for currents up to 7 mA/μm of channel width for a pulse width of 500 ns. MOSFET's with shorter channel lengths require lower voltages to sustain the same current, independent of gate oxide thickness. Increasing the substrate doping does not necessarily reduce the high current voltage. These trends can be explained using a simple lateral n-p-n bipolar transistor snappack model.

I. INTRODUCTION

The high-current snappack characteristics of MOSFET's are an important aspect of the electrostatic discharge (ESD) protection in MOS integrated circuits. ESD stress is usually simulated with the Human Body Model (HBM) which is the discharge of a 100-pF capacitor in series with a 1.5-kΩ resistor. The 100-pF capacitor and 1.5-kΩ resistor represent the human body capacitance and skin resistance, respectively. For a 6-kV HBM stress the (capacitor is charged to 6 kV), a peak current of 4 A with an R-C decay time constant of 150 ns is forced into the ESD protection device. For output pins, the large MOSFET output buffer is often also the ESD protection device [1]. Therefore, the large ESD current is forced into the drain of the output buffer which operates as a lateral n-p-n bipolar transistor in snappack.

To predict ESD failures due to either thermal damage [2] or oxide breakdown [3], the drain voltage, i.e., the high-current I-V of the MOSFET need to be known. Reducing the high-current MOSFET snappack voltage will generally improve the MOSFET's effectiveness against both failure mechanisms. Lower voltages result in lower power dissipation in the device. This leads to lower temperature transients thus reducing the possibility of thermal damage [2]. A lower voltage also reduces the electric field across the thin gate oxides which makes them less likely to suffer breakdown. This is especially important as gate oxide thicknesses continue to decrease to improve transistor performance [3]. Khurana et al. [4] used a transmission line technique to generate very short high-current pulses to measure the I-V without causing thermal damage. Chen [5] showed that the HBM failure voltage can be correlated to the snappack voltage. In this brief, the high-current snappack characteristics of MOSFET's with different channel lengths and widths, gate oxide thicknesses, and substrate dopings are examined.

II. MEASUREMENT TECHNIQUE

The setup used to measure the high-current I-V is shown in Fig. 1. A high-voltage pulse generator provides the necessary voltage and current to cause the grounded-gate MOSFET to operate in its lateral n-p-n bipolar snappack region. The repetitive square pulses have a width of 500 ns or approximately three HBM R-C time constants. This will give a somewhat conservative estimate of the threshold for filamentary conduction. A small duty cycle (1-ms periods) prevents the MOSFET from sustaining any thermal damage during the I-V measurement. The measured I-V characteristics did not change significantly for different pulse widths and duty cycles.

The series resistor (0 to 200 Ω) lowers the minimum measurable current level after snappack for the narrower-channel transistors. A current probe was used to measure the current flowing out of the source and substrate of the MOSFET. Both the current waveform and the voltage waveform at the drain of the MOSFET are stored in a digital oscilloscope. Each I-V data point is the time average of the two waveforms during the high-current stress. The entire I-V characteristic is measured by increasing the high-voltage pulse in a stepwise fashion.

The devices used were conventional (non-LDD, nonsilicide) NMOS transistors with a single poly gate finger as opposed to the ladder structure used for large output transistors. Ladder structures result in nonuniform conduction making their analysis more difficult [6]. LDD transistors have been shown to have higher snappack voltages and correspondingly lower HBM failure thresholds [5].

III. RESULTS AND DISCUSSION

Fig. 2 shows the high-current snappack characteristics of MOSFET's with channel widths of 20, 50, and 100 μm after accounting for the parasitic series resistance of the measurement setup. A BV(10) for the lateral n-p-n bipolar transistor of 7 V is observed for these devices. The increase in voltages for larger currents is believed to be due to high-level injection resulting in a lower effective bipolar current gain (see (1)) and also source/drain series resistances. For currents up to 7 mA/μm of channel width, all three devices lie on the same I-V curve. This suggests that current conduction is uniform across the device width up to this current level as verified by the uniform light emission [7] for the 100-μm-wide transistor (Fig. 2(b)). Stresses greater than 7 mA/μm (500-ns pulse) result in filamentary conduction and device failure. Shorter pulses will have a lower current threshold for filamentary conduction due to thermal considerations. The 7-mA/μm value is higher, even with a longer pulsewidth, than that observed in silicided source/drain devices [6]. This results in a higher ESD failure voltage for conventional transistors [8].

The effect of channel length on the high-current I-V is shown in
Fig. 2. (a) Normalized high-current $I-V$ of MOSFET's with different channel widths. (b) Light emission photograph for the 100-μm-wide transistor for a pulse current stress of 7 mA/μm of device width.

Fig. 3(a). Shorter channel lengths require lower voltages to sustain the same current. This was not observed by the authors of [6] maybe because their range of transistor channel lengths studied were limited to 0.8 to 1.2 μm. However, the snapback voltage dependence on channel length is in agreement with the simple lateral n-p-n transistor snapback model [5], [9]

$$BV_{CEO} = \frac{BV_{CRB}}{(B^*_e)^{2/n}} = \frac{BV_{CRB} (L_{eff})^{2/n}}{L_e}$$  \hspace{1cm} (1)

where $B^*_e = kβ$ is the effective current gain of the lateral bipolar transistor, $L_{eff}$ is the effective channel length, $L_e$ is the electron diffusion length in the p-type substrate, and $n$ is an empirical constant. $B^*_e$ is larger than the measured bipolar $β$ because the lateral bipolar transistor is not externally biased [9]. Using the diode-reverse-recovery technique [10], the minority-carrier lifetime in the substrate is determined to be approximately 150 ns resulting in an $L_e$ of 20 μm. With this value for $L_e$, the $BV_{CEO}$'s of Fig. 3(a) can be fitted to (1) with a reasonable value of $n = 6$ (Fig. 3(b)).

Fig. 4(a) shows the high-current snapback characteristics of MOSFET's with different substrate dopings. A higher substrate doping reduces $BV_{CEO}$ but it also causes $B^*_e$ to decrease. Thus the high-current $I-V$ depends on the sum of these two effects. From the results of [5], Fig. 4(a) suggests that the $4 \times 10^{17}$ cm$^{-3}$ substrate doping transistor will have better ESD performance than the other two transistors. It should be noted that $BV_{CEO}$ is the breakdown voltage associated with the drain and the substrate near the channel, not the usually measured breakdown voltage of the drain/field implanted substrate junction. Fig. 4(b) shows the expected result that the MOSFET gate oxide thickness has no effect on the high-current $I-V$. However, the low-current breakdown leading to MOSFET snapback to $BV_{CEO}$ will depend on the gate oxide thickness [11].

IV. Summary

In this brief, the high-current snapback characteristics of MOSFET's were studied to determine their effectiveness as ESD protection elements. Measurements on different channel width devices show that uniform conduction occurs at least up to a current of 7 mA/μm (500-ns pulse) of device width. Higher current levels re-

Fig. 4. High-current $I-V$ for MOSFET's with different (a) substrate dopings and (b) gate oxide thicknesses.
Influence of Electron Velocity Overshoot on Collector Transit Times of HBT's

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Abstract—Collector transit times of heterojunction bipolar transistors with pronounced electron velocity overshoot effect are investigated based on a simple analytical model. The “effectiveness carrier velocity” \( v_{\text{ref}} \), which is a measure in determining the transit time, is defined as \( \tau_{C} = W_{C}/2v_{\text{ref}} \). It is found that \( v_{\text{ref}} \) is much different from the average velocity \( v_{C} \), which is given by the traveling time through the whole collector depletion layer and the depletion width. With a higher overshoot peak velocity, the collector transit time is shorter than that estimated simply from the average velocity \( v_{C} \).

Reduction in the collector transit time is of great importance in achieving higher cutoff frequencies and faster switching speeds of heterojunction bipolar transistors (HBT's) fabricated with III-V materials. Other delays, such as the base transit time and emitter changing time, can be minimized basically with vertical scale down and increasing collector current. Recently, the tradeoff between the collector transit time and collector capacitance is becoming a major concern. The electron velocity under nonequilibrium conditions can be transiently high, which is a key in relaxing such a constraint. It has already been confirmed that electron velocity overshoot contributes to the reduction in collector transit time [1]–[5]. Because of a relatively small energy separation between the \( \Gamma \) valley and upper L valleys in GaAs, such a contribution is not very large in conventional AlGaAs/GaAs HBT's under practical bias conditions. InP/InGaAs HBT's have been shown to have significant velocity overshoot in the collector due to the higher \( \Gamma \) valley separation [5]. It is also possible to enhance the overshoot effect by tailoring the collector potential profile using, for instance, a ballistic collector transistor (BCT) structure [3], [6]. Of course, the overshoot still depends on the collector bias voltage and the useful bias is limited to a certain range. Consequently, it is thought to be important for the collector design to understand how the overshoot velocity and its width relate to the collector transit time. In this brief, we discuss the collector transit time based on an analytical model with a step-like velocity profile.

The collector transit time \( \tau_{C} \) is determined as a delay of induced output current \( \dot{J}_{\text{out}} \) through the base/collector junction from the particle current \( J \) which is injected from the base into the collector depletion layer. Let us consider the injection current \( J \) having a small signal perturbation with an angular frequency \( \omega \)

\[
J = J_{0} + J_{0} \sin \omega t
\]

where \( J_{0} \) is the dc bias current and \( J_{0} \) is the ac current amplitude. Provided there is no attenuation in the carrier wave due to diffusion, the product of carrier density \( n(x) \) and drift velocity \( v_{D}(x) \) is maintained constant along carrier traveling. That is, a square charge pulse \( \Delta Q \) injected during \( \Delta t \) propagates with a local current density given by \( \Delta Q/\Delta t = qn(x)v_{D}(x) = \text{const.} \). The particle current at position \( x \) is expressed as

\[
J(x) = J_{0} + J(x) = J_{0} + J_{0} \sin \omega t - \int_{y} dy v_{D}(y)
\]

The integral part in the above expression is just the carrier traveling time from the injection point \( x = 0 \) to position \( x \). Total output current density \( \dot{J}_{\text{out}} \) is then given by integrating the sum of \( J(x) \) and displacement current \( \epsilon_{r} \frac{\partial E(x)}{\partial t} \) over depletion width \( W_{C} \)

\[
\dot{J}_{\text{out}} = (1/W_{C}) \int_{0}^{W_{C}} [J(x) + \epsilon_{r} (\partial E(x)/\partial t)] dx = \dot{J}_{\text{out}} + (\epsilon_{r}/W_{C}) \frac{\partial (V_{nc} - V_{BC})}{\partial t}
\]

where \( \epsilon_{r} \) is permittivity, \( E \) is field intensity, \( V_{nc} \) is built-in voltage of the base/collector junction, and \( V_{BC} \) is the base/collector voltage. The first term in (3) is the induced current mentioned above and the second term is a capacitive current through the base/collector junction which provides a source of collector capacitance charging time. Below, the induced current is calculated under some approximations.

For simplicity, we consider here a simplified step-like velocity profile model shown in Fig. 1. Letting \( v_{C} \) and \( v_{D} \) be overshoot velocity and saturation velocity, respectively, \( j(x) \) is expressed in each region as

\[
j(x) = j_{0} \sin \omega (t - x/v_{C}), \quad \text{for } 0 \leq x < W_{c}
\]

\[
j(x) = j_{0} \sin \omega \left[ t - W_{C}/v_{D} - (x - W_{C})/v_{C} \right], \quad \text{for } W_{C} \leq x \leq W_{C} + W_{S}
\]

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