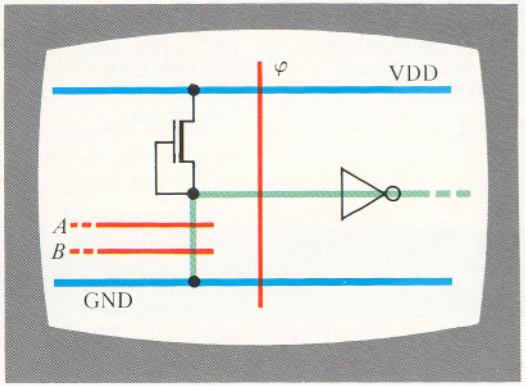
An evaluation tape is available for $100.00 which is applicable to your first month's lease.



VLSI Design

Revolutionizing Your Profession

A Videocourse by
Prof. Carlo H. Séquin
University of California Berkeley

Course materials include:

18 hours of instruction on
22 color videocassettes

Lecture notes—hardcopy of visuals presented on the screen

Textbook—**Introduction to VLSI Systems** by Carver Mead and Lynn Conway

Supplement—**LSI Guide to Implementation** by Robert W. Hon and Carlo H. Séquin

Hellman Associates, Inc.

VLSI Design Videocourse

A Structured Approach to Custom MOS IC Design

VLSI (Very Large Scale Integration) packs 100,000 or more components on a single chip. Unfortunately, designing VLSI chips with conventional IC design techniques is too costly for most custom designs.

New structured design technology now makes low-cost, rapid turnaround, custom IC design available to every system designer. The impact of this new methodology will be as revolutionary as that of microprocessors on digital design.

This new approach allows a computer scientist or a digital design engineer who is unfamiliar with IC design to transfer many of his existing skills to the design of custom ICs, much as high level computer languages such as FORTRAN opened digital computing to a much wider audience. To better serve our clients who wish to attend one of Prof. Séquin's seminars, we have made the entire three day presentation available as a videocourse. This videocourse has been professionally produced to extremely high standards and includes active participation by the viewer.

Intended Audience

The VLSI videocourse is intended for managerial and technical staff concerned with digital circuit design, digital systems design, signal processing or IC design. The only prerequisite is a modest knowledge of programming or digital design. Previous knowledge of IC design or fabrication is **not** required. The seminar evaluates and explains the potential offered by the revolutionary, custom IC design methodology popularized in Mead and Conway's **Introduction to VLSI Systems** which is included in the course materials. Graduated, in class exercises help ensure proper understanding and retention of the material.

"Carlo Séquin was a fantastic lecturer; one of the best I've ever attended." **William Jenkins, US Naval Research Lab.**

"Instructor has an excellent grasp of material. First rate." **Ken Jenkins, General Electric.**

"Dr. Séquin comes across very well on the video—in fact it is one of the best videocourses I have seen—much better than most college videocourses." **Diana Killen, Amdahl Corporation.**

Carlo H. Séquin is known internationally for his pioneering work on VLSI design at Berkeley, Xerox PARC, and Bell Labs. Since 1977 he has been teaching highly popular, interdisciplinary courses that make custom integrated circuit design accessible to computer scientists and systems designers. His research is concerned with the relationship between VLSI and computer architecture, with design methodologies for VLSI systems, and with computer aided design tools for VLSI design. Dr. Séquin's dynamic speaking style is complemented by his on-camera presence. He is currently Professor of EE/CS at the University of California, Berkeley and serves as Chairman of its Computer Sciences Division.

1. The Silicon Revolution and the Need for a New Design Style

Integration—elimination of interfaces
History and trends
Moore's law
*higher density
*higher yield
*design cleverness
The interconnection problem
The complexity barrier
Need for hierarchial design
Why VLSI is different from LSI

58 min.

2. Basic Layout in an Abstract Three Layer Technology

The importance of abstractions
Interlevel contacts
Stick diagrams
Inverter, NAND and NOR gates
And-or-Invert
Charge steering logic
A simple mutiplexor
The tally tree

1 hr. 25 min.

3. Designing Subsystems in Sticks Notation

Logic gates
Programmable logic arrays
Dynamic charge storage
Registers and shift registers
Two-phase clock systems
Mixed notation for subsystems
A LIFO stack subsystem

1 hr. 30 min.

4. Systems Design, Top-down, Bottom-up

Finite state machines
Synchronous systems
Modularity, building blocks
Module generators
PLA layout system
Regularity, arrays of cells

1 hr. 31 min.

5. Real Interconnections and Transistors, IC Fabrication

What does an MOSFET really look like?
The MOS process
Five important mask levels
Fabrication steps
Properties of the three interconnection levels
Resistances and capacitances
Limits of lithography and fabrication

1 hr. 24 min.

6. Other Processes, Mask Layout and Design Rules

PMOS, CMOS, SOS
Future potential of bulk CMOS
Conceptual mask levels
Purpose of design rules
Meta-rules and generalized rules
Geometrical layout rules
Macroscopic layout rules
Electrical design rules

1 hr. 46 min.

7. Electrical Design and Timing

MOS capacitor and transistor
Inverter characteristics
Drive capability, fanout
Distributed delay lines
Using pass transistors
Bus precharging
Types of simulators

1 hr. 44 min.

8. Top-down Chip Design

Arranging the blocks, floor plans
Power and ground nets
Systems partitioning
Packaging considerations
Design for testability
The role of simulation

1 hr. 20 min.

9. The Example of RISC, CAD Tools Used

The Reduced Instruction Set Computer (RISC)
Architectural trade-offs
Procedure call overhead
Overlapping register windows
Size and speed of benchmarks
Floorplan comparisons
RISC register cells
CAD tools used

1 hr. 38 min.

10. The Role of Custom MOS Design

Spectrum of possible approaches
Pros and cons of custom design
Standard cells
Gate Arrays
Module libraries
Mixed approaches
Trade-offs in different design styles
Design systems and environments

51 min.

11. Multiproject Chips, Implementation Services

Sharing of mask and fabrication costs
Multiproject chips
The starting frame
Cell libraries
Implementation services
Silicon foundries

1 hr. 7 min.

12. Description of IC's, the Design-Fabrication Interface

The design-fabrication interface
Transfer levels, required information
CIF, Caltech Intermediate Form
Symbolic IC description formats
Higher level descriptions

1 hr. 42 min.