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299 S. California Avenue
Palo Alto, CA 94306
(415) 328-4091

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VLSI Design

A Structured Approach to Custom MOS IC Design

Palo Alto, CA April 27-29 • Newton, MA June 22-24 • Los Angeles July 13-15

VLSI (Very Large Scale Integration) packs 100,000 or more components on a single chip, promising new economies in electronic circuitry. Improved manufacturing technology will allow VLSI chips to be produced at reasonable prices, but the cost of *designing* such chips is prohibitive using conventional design techniques.

This new, structured design methodology promises to not only relieve that problem, but also to make low cost, rapid turn around, custom IC design available to the system designer. It is predicted that the impact will be as revolutionary as that of high level languages on computer programming, or of microprocessors on digital design.

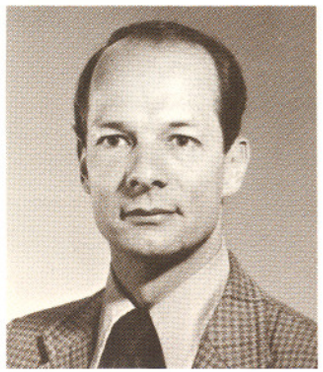
This new approach allows a computer scientist or a digital design engineer who is unfamiliar with IC design to transfer many of his existing skills to the design of custom ICs, much as high level computer languages such as FORTRAN opened digital computing to a much wider audience. At the level of the "silicon compiler" the distinction between programs and high level descriptions of ICs even becomes blurred.

Who Should Attend?

This special seminar is intended for managerial and technical staff responsible for IC design, digital circuit design, digital systems design, or signal processing. It evaluates the potential offered by the new, custom IC design methodology popularized in Mead and Conway's, **Introduction to VLSI Systems** and a copy of this text is included in the course materials. Graduated, in-class exercises help ensure proper understanding and retention of the material. The only prerequisite is a modest knowledge of programming or digital design. Previous knowledge of IC design or fabrication is *not* required.

The nation's top universities, DoD, and industry are scrambling to gain expertise in this new, structured approach to low cost, rapid IC design. Join the IC design revolution by reserving your place now at this intensive special seminar presented by one of the world's leading experts.

"Sequin is great . . . excellent lectures, well prepared . . . very interesting material with a high return for the time invested."



Carlo H. Sequin

Carlo H. Sequin is known internationally for his pioneering work at Berkeley, Xerox PARC, and Bell Labs on VLSI design. Since 1977 he has been teaching highly popular, interdisciplinary courses that make custom integrated circuit design accessible to computer scientists and systems designers. His research is concerned with the relationship between VLSI and computer architecture, with design methodologies for VLSI systems, and with computer aided design tools for VLSI design. Dr. Sequin has authored numerous papers, been awarded several patents and coauthored the first book on Charge Transfer Devices (Academic Press). He is currently Professor of EE/CS at the University of California, Berkeley and serves as Chairman of its Computer Sciences Division.

TOPICS

1. The Silicon Revolution and the Need for a New Design Style

Integration — elimination of interfaces
Exponentially increasing chip functionality
History and trends, Moore's law
- higher density
- higher yield
- design cleverness

The interconnection problem
The complexity barrier
Need for a hierarchical design discipline
The block structured approach to VLSI systems design

2. Basic Layout in an Abstract Three Layer Technology

The importance of abstractions
Three colored layers
Crossing rules and interlevel contacts
Stick diagrams
Inverter, NAND and NOR gates
And-Or-Invert, 2 levels of logic for the price of one
Charge steering logic
A simple multiplexor
The tally tree

3. Designing Subsystems in Sticks Notation

Logic gates
Pass transistors
Dynamic charge storage
Flip-flops
Registers and shift registers
Two-phase clock systems
A LIFO stack subsystem
Layout of programmable logic arrays

4. Synchronous Systems Design

Finite state machines
A design discipline for synchronous systems
Mealy and Moore machines
Higher levels of abstraction
Mixed-mode notation
Modularity, module generators
Very large systems
The synchronization problem, hung flip-flops

5. Real Interconnections and the MOS Transistor

Overview of a simple MOS process
The five important mask levels
The properties of the three interconnection levels
Resistances and capacitances
MOS capacitor
MOS transistor
MOSFET as transmission gate
MOSFET as inverter
Inverter ratio

6. IC Fabrication Technology

The patterning process, photolithography
More detailed description of fabrication steps
- Wafer preparation
- Active area definition
- Transistor formation
- Interlevel contacts
- Interconnections
- Protection

Other related processes
Technological limitations

7. Mask Layout and Design Rules

Meaning of a layout
Purposes of design rules
Layout rules and meta rules
- Limits on mask feature dimensions
- Relative placement of features on different levels
- Macroscopic layout rules

Electrical design rules
- Current limits
- Power dissipation

8. Electrical Design and Simulation

Rise and fall times
Drive capability, fanout
Buffers/drivers
Bus precharging
Using pass transistors
Propagation delays
Distributed delay lines
Current estimates
Power consumption
The role of simulation

9. The Chip Plan

Arranging the blocks
Power and ground nets
Adding clock phases
The direction of metal lines
Pin assignment, bonding pads
Example of a datapath layout
Register cells, barrel shifter, ALU
Testing strategies

10. Standard Languages for the Description of ICs

Design-fabrication interface
- Unambiguous IC descriptions
- Unambiguous acceptance tests

Transfer levels, required information
Standardization efforts
CIF, Caltech Intermediate Form
STIF, Structured Topological Interchange Format
Higher level descriptions
Databases and expert systems

11. Multiproject Chips, Implementation Services

Cost of mask making and wafer fabrication
Cost sharing by combining projects on a chip
Cost sharing by combining chips on a wafer
The starting frame
- Scribe lines
- Alignment marks
- Mask feature test patterns
- Processing test patterns
- Test devices

Cell Libraries
Implementation services
Project schedules

12. The Role of Custom MOS Design

Pros & cons of custom design
Alternative approaches
- Module libraries
- Polycells
- Gate arrays
- Microprocessors

Trade-offs in different design approaches