Homework Assignment #8
Due on bcourses Wednesday 11/11/2020 (zero credit after 9 AM Thursday)

1. [24 pt total] Go to the nanolab homepage and click on Equipment Manual
   a. [1 pt] Roughly how many pieces of equipment are there in the nanolab? (many people, including your professor, will tell you that this is the world’s greatest research clean room. Not so much for the equipment list, as the culture.)
      ~150 pieces of equipment
   b. [12 pts total for part b] Look at the randex manual (6.20).
      i. [1 pt] Look up “randex sputtering system” on google. (the first hit for me was on ebay – you can buy one for $999 – less than a penny on the dollar of the original cost!)
         Roughly how big is this machine?
         About 2mx2mx1m (anything in meters is fine)
      ii. [2 pts] How many different targets are there? How many are dielectrics?
           31 Targets and 9 dielectrics: Al₂O₃, Flint Glass, ITO (actually a conductor), LiF, MgO, SiO₂, SnO₂, (actually a semiconductor), Tantalum Oxide, 7059 Glass
           no points off for +/- 1 or 2, or mistakes on identifying dielectrics
      iii. [1 pt] What is the upper limit on the baseline pressure for the system before starting to etch (ion gauge reading, 8.3.3)?
          3x10⁻⁶ Torr
      iv. [2 pt] If the system were at max baseline pressure with only oxygen in the chamber, how many monolayers per second of oxide growth would there be?
          Max baseline pressure is 3μTorr and in class 1monolayer/sec for 1μTorr was given, so 3 monolayer/sec for 3μTorr
      v. [2 pt] What is the maximum power for dielectric targets? Why is it less than metal targets?
         300 watts because the poor thermal conductivity of dielectrics heat is not effectively transferred to the coolant and the target may crack when cooling down due to differential cooling
      vi. [4 pt] What is a typical deposition rate (Table 1)? Roughly how many monolayers per second does this correspond to? How does that compare to your oxide growth answer? Why is that important?
          [1 pt] ~200A/min for the conductors (fine if you picked anywhere 150-400A/min)
          [1 pt] ~3 A/monolayers
          [1 pt] This is ~1/3 of the oxide growth calculated...not good!
          [1 pt for any attempt at an explanation] BUT. Our oxygen calculation assumes there’s “only oxygen in the chamber.” Oxygen is only 21% in atmosphere so there is a factor of 5 just air brought down to max baseline pressure and other gases can be flow to make that percentage even lower. Also, oxygen gets “gettered” – meaning what little there is reacts very quickly in
          It’s important to have a higher deposition rate than oxide so that you’re putting down the material you expect to, not it’s oxide
      c. [2 pt] Take a look at the NRC thermal evaporator (6.35)
         i. How many different materials are allowed for evaporation?
            14 materials (Ag, Al, Au, Co, Cr, Cu, Fe, In, Ni, Pd, Si, Sn, Ti, ITO)
         ii. What is the base pressure of the vacuum pump? What is the mean free path of air at this pressure?
            7 x 10⁻⁷ Torr
            In class 50m was given for for 1μTorr so ~70m because the mean free path is \( \frac{1}{\text{pressure}} \)
      d. [9 pt] Check out Technics-C. Your professor used this exact same tool a lot when he was a graduate student, probably before you were born.
         i. [4 pt] What are the available processes, and what are they used for?
Oxygen Scourge: Use this procedure to clean the chamber before doing any SF6 nitride etching.

Descum: This is used after developing exposed photoresist, before hard baking, to eliminate any residual scum.

Resist Stripping or Ashing: For complete removal of standard hard baked G and I-line photoresist.

Nitride Etch: etching nitride

ii. [5 pt, 1 each for process, gas, and etch rates] Etching silicon is not listed as an available process, but one of the etches says it will etch silicon. What process is that? What gas? What is the etch rate of silicon, silicon dioxide, and silicon nitride in this process?

The Nitride etch will etch Si with SF6. It etches Si at 8000A/min, Nitride at 500 – 600 A/min and Oxide at 200 – 300 A/min

Note that even though this is called a nitride etch, it actually etches silicon more than ten times faster than nitride!

2. [6 pts] Check out the characterization of the Stanford DRIE machine [1]
   a. [1 pt] Estimate the etch depth per pulse in the cross-section figure on slide 6. Is that rate consistent with the depth per pulse that can be calculated from the data provided in the text on the left? And with the undercut?
      From the text on slide 6: 65 cycles in 6 minutes and 4.5um/min so 415nm/cycle
      The slide and question didn’t match, so give yourself a point for any answer here.
   b. [1 pt] With the recipe on slide 6, how thick would the photoresist need to be to etch all the way through a 760um thick wafer (about the thickness of a standard 300mm wafer)?
      76:1 selectivity means for every 76(um, nm, m, etc.) Si is etched, PR is etched 1(um, nm, m, etc.) so at least 10um of PR is needed to etch through 760um
   c. [1 pt] from the figures on slide 7, which rank the following by etch rate from fastest to slowest: trenches that are 7um and 12um wide, and holes that are 7, 10, and 12um wide. Very roughly, what’s the percent difference in etch rate for a 7um hole vs. a 7um trench?
      Roughly 15% increase in etch rate for a trench
   d. [1 pt] Look at slide 15 and cry a little imagining that this is your project/product. What process might get rid of the grass once it’s grown?
      A quick Si isotropic etch like XeF2
      An isotropic etch works to get rid of the grass because though it may be tall, it’s typically very thin so an isotropic etch will quickly remove it because it attacks all directions uniformly
   e. [2 pts] Estimate the variation in sidewall angle vs. trench width in slide 16.
      [1 pt] The sidewall for the 5um trench looks pretty close to 90%, although it isn’t super straight.
      [1 pt] The angle gets larger (fatter etch pit) as the trench mask width gets wider. It looks like it’s several degrees from vertical for the 200 um etch.

3. [4 pt] In an RF plasma etching system with only Argon as a feed gas,
   a. [1 pt] is the etching done primarily by chemical processes, or kinetic?
      kinetic
   b. [1 pt] Would you expect the etch to be isotropic, or anisotropic with vertical sidewalls?
      anisotropic with vertical sidewalls because it’s kinetic: shoots down and not having reactants react with substrate in every direction
   c. [1 pt] Would you expect the etch to have good selectivity between silicon and other materials?
      No. It’s bombarding all materials and since it’s not a chemical process, it’s physically dislodging material, it’s less selective
   d. [1 pt] Would you expect that the wafer would be on the grounded electrode, or the capacitively isolated electrode?
      Give yourself 1 pt for any answer. What I was looking for is that if it is doing any etching with Argon it must be using sputtering, which means that the wafer would be floating (capacitively isolated, to generate a negative bias). But usually when people say “plasma etcher” they mean that the wafer is grounded, so the question was a bit confusing.

4. [5 pt] In the Bosch Deep RIE process, your friend from Stanford says that the vertical etch profiles are due to really fast reactive ions digging straight into the silicon surface.
   a. [1 pt] Do you agree?
      No. The vertical etch profiles are due to the passivation step coupled with the semi directed etch
b. [2 pt] Is the silicon etching primarily due to chemical etching, or kinetic? How can you tell from looking at the etched cross-section?
c. [1 pt] Would you expect the silicon etch to be very selective to other materials, somewhat selective, or not selective?
  Very selective since its primarily chemical.
d. [1 pt] What prevents lateral etch due to reactive neutrals?
  Conformal passivation (Teflon-like film) between etch cycles helps to prevent lateral etching.
5. [1 pt] What would happen in an LPCVD tube being fed with silane and oxygen if the process were run at atmospheric pressure instead of low pressure?
  It explodes.
6. [18 pt] Of the following process steps: thermal oxidation; parylene deposition (see nanolab manual); LPCVD LTO, PSG, polysilicon, silicon nitride; which can be used with a wafer that has
  a. aluminum on it; b. photoresist on it; c. polysilicon on it

<table>
<thead>
<tr>
<th>Thermal oxidation</th>
<th>Aluminum</th>
<th>Photoresist</th>
<th>polysilicon</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parylene deposition</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LTO</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PSG</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>POLY</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>nitride</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Thermal oxidation is done at a “high temperature”: easily 800°C but generally at or above 1000°C
  Parylene Deposition: 25°C
  LPCVD LTO: 425°C
  LPCVD PSG: 450°C
  LPCVD polysilicon: 580°C-625°C
  LPCVD silicon nitride: done at 835°C

Aluminum eutectic formation with Si: 450°C
  Photoresist Melting Point: Depends on the PR. Tons of types all with different properties. Generally want to keep it below 100°C
  Polysilicon <1400°C

With this info you can see which depositions are allowed given each material that is already on the wafer. 1 pt each

7. [1 pt] Referring to the CMOS-MEMS powerpoint presentation on the course website,
  a. [3 pts] What is the material etched, and what defines the region to be etched, in the figure on slide 4?
     What materials can be included in the remaining structures?
     Silicon is etched. SiO₂ defines the region to be etched in addition to the 111 Si planes.
     SiO₂ can be included in the remaining structure
  b. [8 pts] What is the material etched, and what defines the region to be etched, in Figure b on slide 5? Figure c? Figure d? What materials can be included in the remaining structures?
     [2 pts] Silicon Oxide is etched, and the shape is defined by the gaps in the metal traces anisotropically
     c. [2 pts] Silicon is etched, and the shape is defined by the metal and/or the silicon oxide trenches anisotropically
     d. [2 pts] Silicon is etched, and the shape is defined by the Silicon trenches isotropically.
     [2pts] Metal, silicon oxide, 1 pt each (and polysilicon) are included in the remaining structure
  c. [12 pt] What is the material etched, what is the etchant used, and what defines the region to be etched, between Figures a and b on slide 7? Between Figures b and c? Between Figures c and d? What materials can be included in the remaining structures?
[3 pts] a to b: Aluminum and Tungsten etched by H₂SO₄ + H₂O₂ (piranha) defined by passivation
[3 pts] b to c: all passivation is removed by RIE. No masking.
[3 pts] c to d: Si etched with XeF$_2$ defined by the gaps from the removed Al and Tu
[3 pts] Aluminum, Tungsten, Silicon Oxide, and Poly (1 pt each, up to 3 pts)
d. [3 pts] What is the material etched, and what defines the region to be etched, on slide 9? What
materials can be included in the remaining structures?
[2 pts] Oxide is etched defined by aluminum and passivation via an isotropic etch
[1 pt] The remaining structure is aluminum (ok to add oxide and passivation)

8. [4 pts] In the Nasiri CMOS+MEMS process used by Invensense
   a. [1 pt] What is the MEMS structural layer?
      Silicon
   b. [1 pt] What is the sacrificial layer? (this is a trick question)
      There is no sacrificial layer.
   A sacrificial layer is one that is deposited, only to later be completely removed. Typically it’s purpose is to create
gaps, like the Si oxide in PolyMumps
   c. [2 pts] What materials are used in the bond that provides electrical connection between the
      CMOS and MEMS devices, and provides a vacuum seal as well?
      Aluminum and Germanium

9. [2 pts] In the Nasiri process,
   a. [8 pts] Sketch the layout that would give a 1mm$^2$ sealed cavity. Show specifically the layers
      used on both CMOS and MEMS substrates, and draw a representative cross-section. For the
      CMOS, assume the top layer is M5, and that the overglass cut mask is called OG.

You should have four figures. 2 pts for each figure. The MEMS wafer can also have a cavity. For this problem
you only needed a sealed cavity so the important aspects are the CMOS cross section and the GERMANIUM, and
STANDOFF, plus the STRUCT needs to be larger than the CMOS CAVITY. Having a MEMS CAVITY is fine.
Need to show an aluminum ring on the CMOS wafer, and a Germanium ring on the MEMS wafer

b. [8 pts] Sketch the layout for two electrically-isolated contacts between CMOS and MEMS
devices. Show specifically the layers used on both CMOS and MEMS substrates, and draw a
representative cross-section.
c. [8 pts] Using your answers above, sketch a very simple vacuum-packaged differential capacitive accelerometer.

Give yourself a point for each figure if you drew anything at all. Full credit if you got close.

10. [6 pts] In the Intel 22nm CMOS process [2], Figures 1 and 2 show drawings and electron micrographs of FINFET transistors (invented and patented at Berkeley).

   a. [2 pts] There are at least a dozen transistors in the upper right picture. The gates and fins are on 60nm centers - how big is the central array? How does that compare to a minimum-sized feature in polyMUMPS?

   About 250nm x 350nm which is 1/8 to 1/6 of Polymumps minimum 2um feature. You could fit a *lot* of transistors on the most narrow polymumps beam.

   b. [4 pts] Figure 16 shows an electron micrograph of the metalization stack with 10 layers of metal wiring above a layer of FINFETs. Assuming that the 1x layers have an 80nm pitch,

      i. [2 pts] what is the width and height of the picture

      width: 19x80nm=1520nm=1.52um

      height: ~3um

      ii. [2 pts] what is the longest wire that you could draw on a 1x layer on a 1cm2 chip?

      Assume trace width is the same as pitch. That's pretty standard.

      How many vertical lines? \( \frac{1\text{cm}}{160\text{nm}} = 62500 \)
1 cm trace long repeated 62500 times
Longest wire on 1x layer is 625m. WOAH! Almost a kilometer.

11. [ee247A] Pick a project topic, and write down detailed captions for at least five figures that you'd like to see in your final paper.