Instruction		*j*	*k*	*iteration*	*Read*	*Executior*	*Write*	*Code:*			
LD	F2	0	R1	1	*Issue*	*operand*	*complete*	*Resul*	LD	F2	0 R1
MULTD	F4	F2	F0	1					MULTI	F4	F2 F0
LD	F6	0	R2	1					LD	F6	0 R2
ADDD	F6	F4	F6	1					ADDD	F6	F4 F6
SD	F6	0	R2	1					SD	F6	0 R2
LD	F2	0	R1	2					ADDI	R1	R1 #8
MULTD	F4	F2	F0	2					ADDI	R2	R2 #8
LD	F6	0	R2	2					SGTI	R3	R1 done
ADDD	F6	F4	F6	2					BEQZ	R3	foo
SD	F6	0	R2	2							

Functional unit status			*dest*	*S1*	*S2*	*FU,j*	*FU,k*	*Fj?*	*Fk?*
Time	*Name*	*Busy* *Op*	*Fi*	*Fj*	*Fk*	*Qj*	*Qk*	*Rj*	*Rk*
	Integer1								
	Integer2								
	Integer3								
	Mult1								
	Mult2								
	Add								
	Divide								

Register result status												
Clock	**R1**	**R2**	*F0*	*F2*	*F4*	*F6*	*F8*	*F10*	*F12*	...	*F30*
0	**0**	**0**	*FU*								

Instruction		*j*	*k*	*iteration*	*Read*	*Executior*	*Write*	*Code:*			
LD	F2	0	R1	1	*Issue operand*	*complete*	*Resul*	LD	F2	0	R1
MULTD	F4	F2	F0	1				MULTI	F4	F2	F0
LD	F6	0	R2	1				LD	F6	0	R2
ADDD	F6	F4	F6	1				ADDD	F6	F4	F6
SD	F6	0	R2	1				SD	F6	0	R2
LD	F2	0	R1	2				ADDI	R1	R1	#8
MULTD	F4	F2	F0	2				ADDI	R2	R2	#8
LD	F6	0	R2	2				SGTI	R3	R1	done
ADDD	F6	F4	F6	2				BEQZ	R3	foo	
SD	F6	0	R2	2							

Functional unit status					*dest*	*S1*	*S2*	*FU,j*	*FU,k*	*Fj?*	*Fk?*
	Time	*Name*	*Busy*	*Op*	*Fi*	*Fj*	*Fk*	*Qj*	*Qk*	*Rj*	*Rk*
		Integer1									
		Integer2									
		Integer3									
		Mult1									
		Mult2									
		Add									
		Divide									

Register result status

Clock	**R1**	**R2**		*F0*	*F2*	*F4*	*F6*	*F8*	*F10*	*F12*	...	*F30*
0	**0**	**0**	*FU*									

Instruction		*j*	*k*	*iteration*	*Read*	*Execu*	*Write*	*Code:*			
LD	F2	0	R1	1	*Issue*	*opera*	*comp*	*Resul*	LD	F2	0 R1
MULTD	F4	F2	F0	1					MULTD	F4	F2 F0
LD	F6	0	R2	1					LD	F6	0 R2
ADDD	F6	F4	F6	1					ADDD	F6	F4 F6
SD	F6	0	R2	1					SD	F6	0 R2
LD	F2	0	R1	2					ADDI	R1	R1 #8
MULTD	F4	F2	F0	2					ADDI	R2	R2 #8
LD	F6	0	R2	2					SGTI	R3	R1 done
ADDD	F6	F4	F6	2					BEQZ	R3	foo
SD	F6	0	R2	2							

Functional unit status				*dest*	*S1*	*S2*	*FU,j*	*FU,k*	*Fj?*	*Fk?*
Time	*Name*	*Busy*	*Op*	*Fi*	*Fj*	*Fk*	*Qj*	*Qk*	*Rj*	*Rk*
	Integer1									
	Integer2									
	Integer3									
	Mult1									
	Mult2									
	Add									
	Divide									

Register result status											
Clock	**R1**	**R2**		*F0*	*F2*	*F4*	*F6*	*F8*	*F10*	*F12*	... *F30*
0	**0**	**0**	*FU*								

Instruction		*j*	*k*	*iteration*	*Read*	*Execu*	*Write*	*Code:*			
LD	F2	0	R1	1	*Issue*	*opera*	*comp*	*Resul*	LD	F2	0 R1
MULTD	F4	F2	F0	1					MULTD	F4	F2 F0
LD	F6	0	R2	1					LD	F6	0 R2
ADDD	F6	F4	F6	1					ADDD	F6	F4 F6
SD	F6	0	R2	1					SD	F6	0 R2
LD	F2	0	R1	2					ADDI	R1	R1 #8
MULTD	F4	F2	F0	2					ADDI	R2	R2 #8
LD	F6	0	R2	2					SGTI	R3	R1 done
ADDD	F6	F4	F6	2					BEQZ	R3	foo
SD	F6	0	R2	2							

Functional unit status	*dest*	*S1*	*S2*	*FU,j*	*FU,k*	*Fj?*	*Fk?*

Time	*Name*	*Busy*	*Op*	*Fi*	*Fj*	*Fk*	*Qj*	*Qk*	*Rj*	*Rk*
	Integer1									
	Integer2									
	Integer3									
	Mult1									
	Mult2									
	Add									
	Divide									

Register result status

Clock	**R1**	**R2**		*F0*	*F2*	*F4*	*F6*	*F8*	*F10*	*F12*	...	*F30*
0	**0**	**0**	*FU*									