CS152
Computer Architecture and Engineering
Lecture 1

January 18, 1995

Dave Patterson & Shing Kong

Overview of Today's Lecture

- Course Overview (20 minutes: Dave Patterson)
- Administrative Matters (3 minutes: DP)
- Course Philosophy and Structure (10 min: DP)
- Level of Representation (15 min: DP)
- Break (5 min)
- Levels of Organization (25 min: Kong)

CS152: Course Overview

Computer Design

Instruction Set Deign
- Machine Language
- Compiler View
- "Computer Architecture"
- "Instruction Set Processor"

"Building Architect"

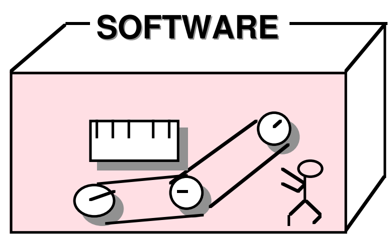
Computer Hardware Design
- **Machine Implementation**
- Logic Designer's View
- "Processor Architecture"
- "Computer Organization"

"Construction Engineer"

Instruction Set Architecture

. . . the attributes of a [computing] system as seen by the programmer, i.e. the conceptual structure and functional behavior, as distinct from the organization of the data flows and controls the logic design, and the physical implementation.

Amdahl, Blaaw, and Brooks, 1964



-- Organization of Programmable Storage

-- Data Types & Data Structures: Encodings & Representations

-- Instruction Formats

-- Instruction (or Operation Code) Set

-- Modes of Addressing and Accessing Data Items and Instructions

-- Exceptional Conditions

Organization

ISA Level

FUs & Interconnect

Logic Designer's View

-- Capabilities & Performance Characteristics of Principal Functional Units

(e.g., Registers, ALU, Shifters, Logic Units, etc.

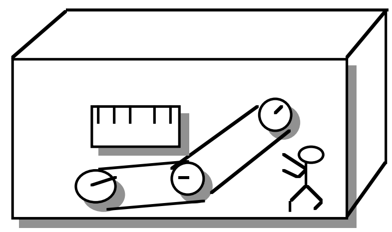
-- Ways in which these components are interconnected

-- nature of information flows between components

-- logic and means by which such information flow is controlled.

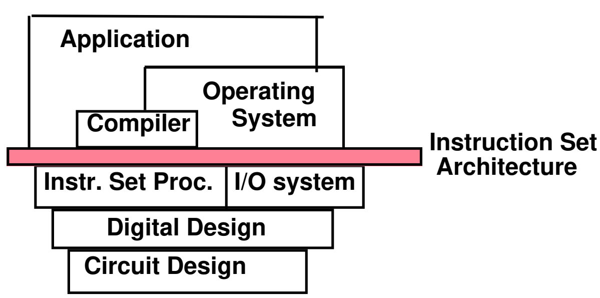
Choreography of FUs to realize the ISA

Register Transfer Level Description



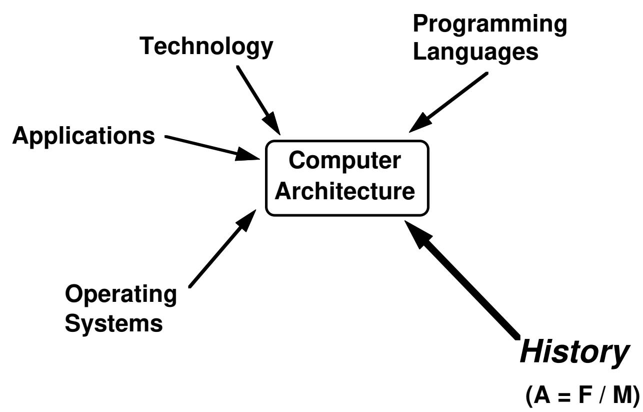
What is "Computer Architecture"

° Co-ordination of *levels of abstraction*

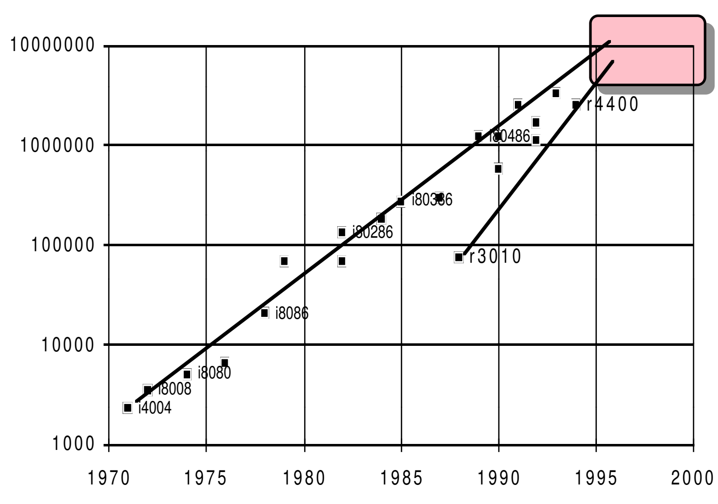


° Under a set of rapidly changing *Forces*

Forces on Computer Architecture

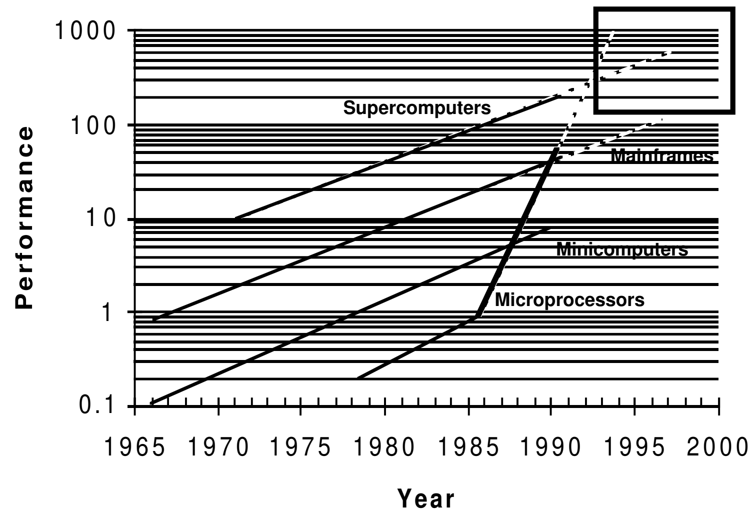


Technology: Microprocessor Logic Density

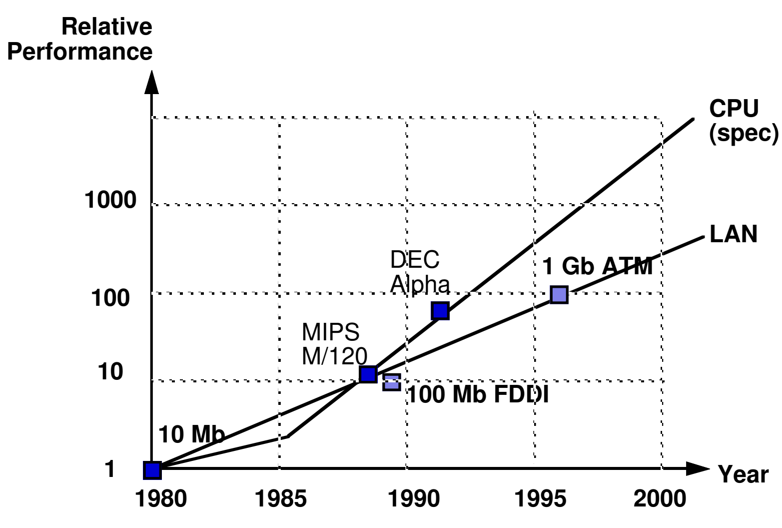


Memory: 4x every 3 years

Performance Trends



CPU and LAN Performance



Levels of Representation

High Level Language Program

temp = v[k];
v[k] = v[k+1];
v[k+1] = temp;

Compiler

Assembly Language Program

lw $15, 0($2)
lw $16, 4($2)
sw $16, 0($2)
sw $15, 4($2)

Assembler

Machine Language Program

Machine Interpretation

Control Signal Spec

MIPS R3000 Instruction Set Architecture

- **Instruction Categories**
  - **Load/Store**
  - **Computational**
  - **Jump and Branch**
  - **Floating Point**
    - **coprocessor**
  - **Memory Management**
  - **Special**

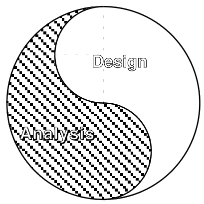
R0 - R31

PC
HI
LO

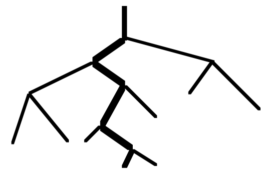
Instruction Format

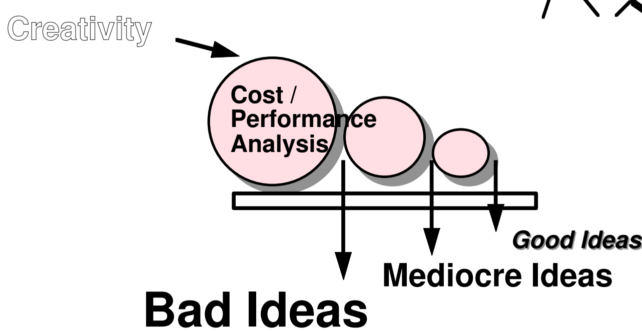
OP	rs	rt	rd	sa	funct
OP	rs	rt	immediate		
OP	target				

Measurement and Evaluation



Architecture is an iterative process
-- searching the space of possible designs
-- at all levels of computer systems





CS152: Course Overview (cont)

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Construction Engineer

Few people design computers! Very few design instruction sets!
Many people design computer components.
Very many people are concerned with computer function, in detail.

CS152:So what's in it for me?

- In-depth understanding of the inner-workings of modern computers, their evolution, and trade-offs present at the hardware/software boundary.
  - Insight into fast/slow operations that are easy/hard to implementation hardware
- Experience with the *design process* in the context of a large complex (hardware) design.
  - Functional Spec --> Control & Datapath --> Physical implementation
  - Modern CAD tools
- Designer's "Intellectual" toolbox.

CS152: Computer Architecture and Engineering

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Text: Computer Organization & Design

The Hardware / Software Interface

Course Philosophy

- Lecture style
  - 20-Minute Lecture
  - 3- Minute Administrative Matters
  - 25-Minute Lecture
  - 5-Minute Break
  - 25-Minute Lecture
- Reduce the workload of the class
  - Final project has been simplified
  - Lab 3 - 6 are directly related to the project
  - Project teams must have at least 4 members
  - No final exam. Only Two mid-terms.
- Reduce the pressure of taking exams
  - Both mid-terms will be open book
  - You will have 3 hrs to take the 2-hr test (5-8 PM, Sibley Auditorium)
  - Our goal: test your knowledge

Simulate Industrial Environment

- Project teams must have at least 4 members
- Communicate with colleagues (team members)
  - What have you done?
  - What answers you need from others?
  - You must document your work!!!
  - Everyone must keep an on-line notebook
- Communicate with supervisor (TAs)
  - How is the team's plan?
  - Short progress reports are required:
    - What is the team's game plan?
    - What is each member's responsibility?

Course Structure

° **Design Intensive Class --- 75 to 150 hours per student**

MIPS Instruction Set ---> Standard-Cell implementation

° **Modern CAD System (VIEW*logic*):**

Schematic capture and Simulation

Design Description

Computer-based "breadboard"
- **Behavior over time**
- **Before construction**

° **Lectures:**
- **1 week on Overview**
- **2 weeks on ISA Design**
- **5 weeks on Proc. Design**
- **4 weeks on Memory and I/O**
- **3 weeks on special topics**

Homework Assignments and Project

° **Each assignment consists of two parts**
- **Individual Effort: Exercises from the text book**
- **Team Effort (After Lab 3): Lab assignments**

° **All assignments are assigned on Friday and due on a later Monday**

° **Here is the list of lab assignments:**
- **Lab 1 Measure real machines' performance (1 week)**
- **Lab 2 MIPS R3000 ISA and SPIM (2 weeks)**
- **Lab 3 ALU Design (2 weeks)**
- **Lab 4 Single Cycle Processor Design (2 weeks)**
- **Lab 5 Pipelined Processor Design (4 weeks - 1 week Spr. Break)**
- **Lab 6 Cache Design (2 weeks)**

° **Final project: Integrate Lab 5 and Lab 6 together**

° **Safety Net: Cache modules will be provided**

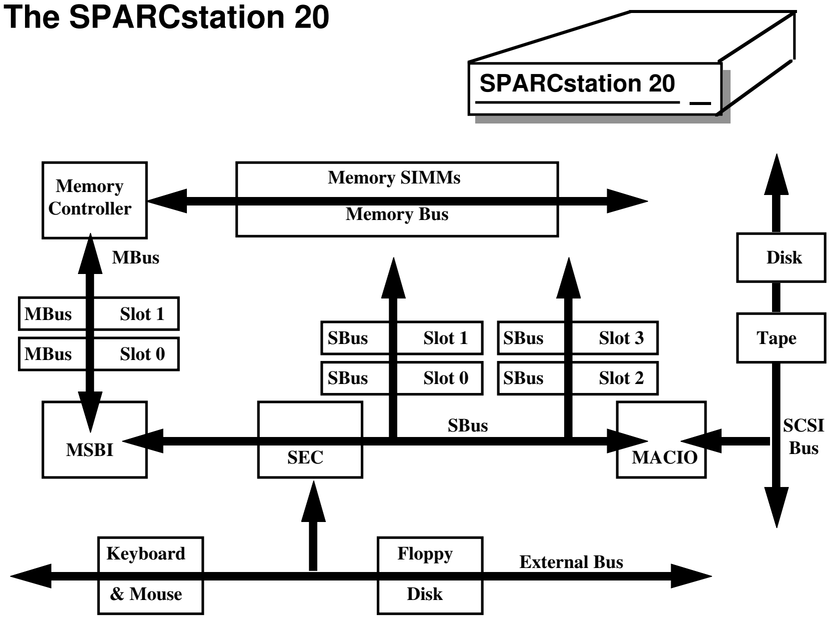
Course Problems

- No late homeworks or labs (except for lab 5)
- What is cheating?
  - Studying together in groups is encouraged
  - Work must be your own
  - Common examples of cheating: running out of time on a assignment and then pick up output, take homework from box and copy, person asks to borrow solution “just to take a look”, copying an exam question, ...

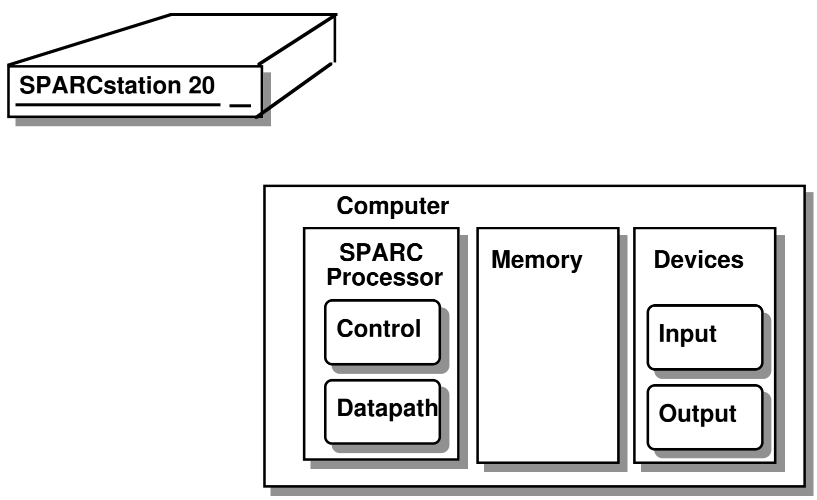
Decide on penalties for cheating

- Exercises (book):
  - 0 for problem
  - 0 for homework assignment
  - subtract full value for assignment
  - subtract 2X full value for assignment
- Labs leading to project (groups: only penalize individuals?)
  - 0 for problem
  - 0 for homework assignment
  - subtract full value for assignment
  - subtract 2X full value for assignment
- Exams
  - 0 for problem
  - 0 for exam

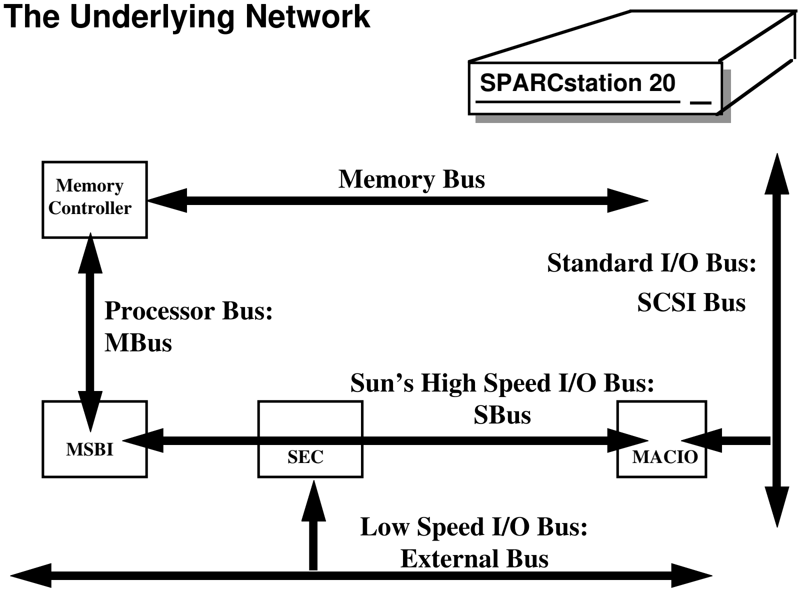
The SPARCstation 20



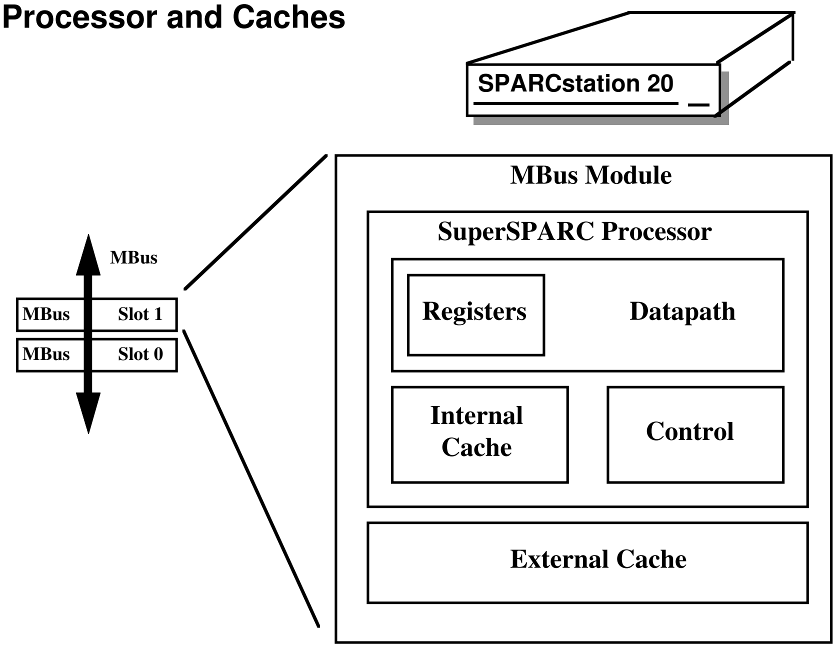
Levels of Organization



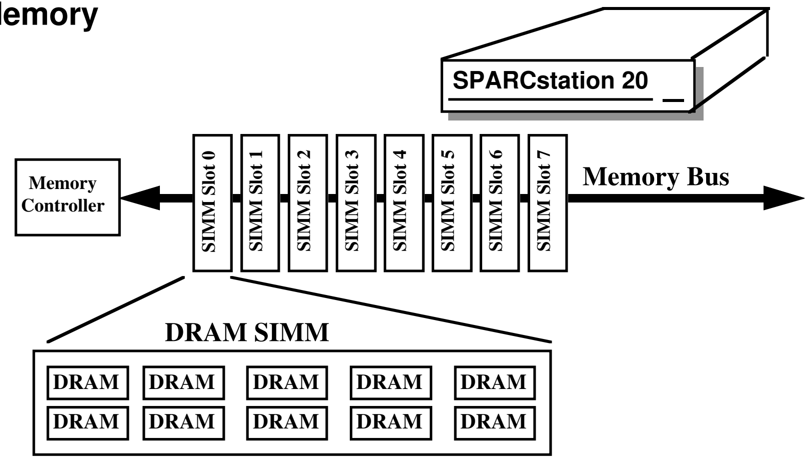
The Underlying Network



Processor and Caches

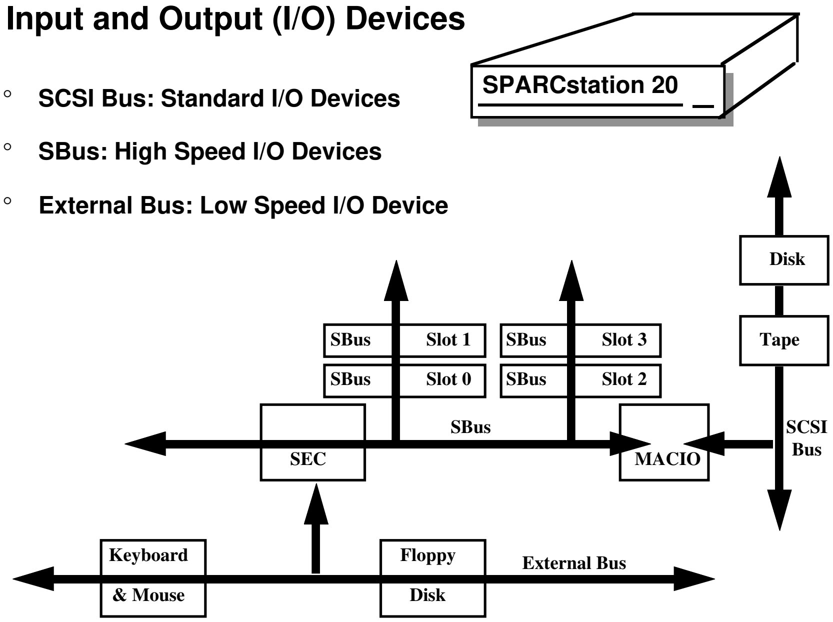


Memory

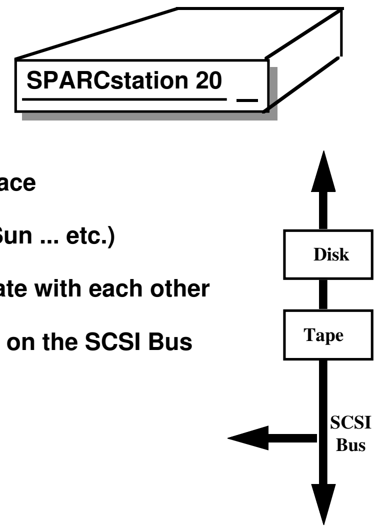


Input and Output (I/O) Devices

- SCSI Bus: Standard I/O Devices
- SBus: High Speed I/O Devices
- External Bus: Low Speed I/O Device

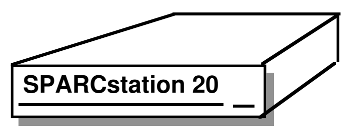


Standard I/O Devices

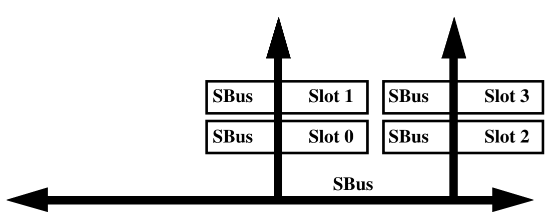


- SCSI = Small Computer Systems Interface
- A standard interface (IBM, Apple, HP, Sun ... etc.)
- Computers and I/O devices communicate with each other
- The hard disk is one I/O device resides on the SCSI Bus

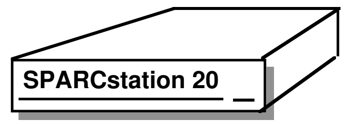
High Speed I/O Devices



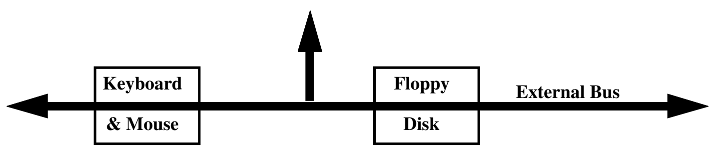
- SBus is SUN's own high speed I/O bus
- SS20 has four SBus slots where we can plug in I/O devices
- Example: graphics accelerator, video adaptor, ... etc.
- High speed and low speed are relative terms



Slow Speed I/O Devices



- The are only four SBus slots in SS20--”seats” are expensive
- The speed of some I/O devices is limited by human reaction time--very very slow by computer standard
- Examples: Keyboard and mouse
- No reason to use up one of the expensive SBus slot



Summary

- All computers consist of five components
  - Processor: (1) datapath and (2) control
  - (3) Memory
  - (4) Input devices and (5) Output devices
- Not all “memory” are created equally
  - Cache: fast (expensive) memory are placed closer to the processor
  - Main memory: less expensive memory--we can have more
- Input and output (I/O) devices has the messiest organization
  - Wide range of speed: graphics vs. keyboard
  - Wide range of requirements: speed, standard, cost ... etc.
  - Least amount of research (so far)