Area-Performance Trade-offs in Tiled Dataflow Architectures

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Overview

- WaveScalar is a dataflow architecture, that can also execute conventional programs*
- This paper compares tradeoffs in area for performance

Dataflow Background

```
int *V;
int a, b;
int c, d, r;
r = a*c + b*d;
forall a = 2*r + d <= 2;
```

WaveScalar Architecture

- Dynamic dataflow with tagged-tokens
- Wave-ordered memory allows it to execute programs with conventional von Neumann-style memory operations
PE Pipeline

- PE - Processing Element
- Pod - 2 PE's - ALU's share bypass
- Domain - Group of pods that communicate by pipelined bus
- Cluster - 4 domains, L1 data, network switch, and store buffer

Network

- Hierarchical - different network for each organization unit
- Intra-pod - bypass from ALU's
- Intra-domain - broadcast, claim light traffic
- Intra-cluster - switched point-to-point
- Inter-cluster - routed, 6 ports (4 to other clusters, 2 internal)

Experimental Setup

- Objective is try out many possible configurations and measure their performance/area
- RTL Model made with current synthesis tools to get area estimates and make area model
- Cycle-Accurate Simulator used to get performance of each design
Experimental Setup

- Workload
  - Multi-threaded - SPLASH 2
  - Single-threaded - SPECInt, SPECFP, Mediabench
- Full parameter space too big, cut out unbalanced and infeasible designs

Parameters Explored

<table>
<thead>
<tr>
<th>Variable</th>
<th>Description</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td># of clusters</td>
<td>1-64</td>
</tr>
<tr>
<td>D</td>
<td># of domains per cluster</td>
<td>1-4</td>
</tr>
<tr>
<td>P</td>
<td># of PE's per domain</td>
<td>2-8</td>
</tr>
<tr>
<td>V</td>
<td>instruction capacity per PE</td>
<td>8-256</td>
</tr>
<tr>
<td>M</td>
<td># of matching table entries</td>
<td>16-128</td>
</tr>
<tr>
<td>L1</td>
<td>cache per cluster</td>
<td>8-32KB</td>
</tr>
<tr>
<td>L2</td>
<td>total L2 cache</td>
<td>0-32MB</td>
</tr>
</tbody>
</table>

Evaluation

- AIPC = Alpha instructions per cycle

Optimal Tradeoffs

- SPLASH Insights
  - Single-cluster designs limited by L1
  - Changing large L1 for L2 gave big boost
  - More clusters (and thus more PE's) lead to need for lower virtualization degrees
- Single-threaded had trouble using more area
Comparison to Others

• Alpha EV7 - scaled for modern process and normalized cache sizes
  • WaveScalar design of equivalent performance uses a third of the area
• Niagara I (with single-threaded workload)
  • Worst WaveScalar design is twice as efficient per area

Questions?