Investigation of Interconnect Capacitance Characterization Using Charge-Based Capacitance Measurement (CBCM) Technique and Three-Dimensional Simulation

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Abstract—This paper examines the recently introduced charge-based capacitance measurement (CBCM) technique through use of a three-dimensional (3-D) interconnect simulator. This method can be used in conjunction with simulation at early process development stages to provide designers with accurate parasitic interconnect capacitances. Metal to substrate, interwire, and interlayer capacitances are each discussed and overall close agreement is found between CBCM and 3-D simulation. Full process interconnect characterization is one possible application of this new compact, high-resolution test structure.

Index Terms—Capacitance measurement, CMOS integrated circuits, integrated circuit interconnections, integrated circuits measurements, monitoring, test structures.

I. INTRODUCTION

In the past, circuit delay has been due mostly to transistors. For this reason, much effort is put into device scaling. Today, the dominant source of delay in circuits such as ASIC’s and microprocessors is metal interconnect. According to the Semiconductor Industry Association’s Roadmap [1], metal 1 RC wiring delay will increase by over 900% from the 0.35-μm to the 0.1-μm generation. During the same time interval, gate delays drop from 70 ps to 20 ps while the clock period is reduced by 70%. As interconnect scales with each technology generation, several tradeoffs are made. In order to reduce line resistance and improve electromigration properties, metal height is kept fairly constant and not scaled with pitch. The increasing aspect ratio (height/width) results in larger coupling capacitances and more crosstalk. This problem worsens as more metal layers are added with almost every generation. The performance gains of adding more metallization layers will soon saturate; in other words, a limit exists for the number of metal layers feasible for integrated circuits. Once this limit is reached, only tighter pitches in each layer will result in higher density, leading to larger capacitances again [2].

From these points, it can be seen that interconnect capacitance characterization is an important aspect of current and future process development as well as circuit design. In order to give circuit designers an accurate assessment of speed and noise issues, parasitic capacitances due to interconnect must be well described. Currently, this is done with extensive computer simulations. A new, measurement-based technique, charge-based capacitance measurement (CBCM) [3], has been developed to characterize interconnect capacitances. This simple, compact, and sensitive test structure can be used to measure any interconnect capacitance structure. In this paper, we will compare the results from CBCM to those obtained by RAPHAEL, a capacitance simulation package [4].

II. METHODOLOGY

A test chip was fabricated in a production 0.8-μm, double-metal technology with many interconnect test structures. An example of the test structure used is shown in Fig. 1. \( V_1 \) and \( V_2 \) are nonoverlapping waveforms that can be generated either on-chip or off-chip that serve to eliminate short-circuit current as a potential source of error in the measurement. The difference between the measured currents \( I \) and \( I' \) will be directly proportional to the capacitance being measured as well as the frequency of operation and the supply voltage as expressed in (1) and (2)

\[
I - I' = I_{\text{ref}} \\
I_{\text{ref}} = CV_{\text{dd}}f.
\]

The measurement setup itself is very simple; only a dc ammeter is required to yield the average current supplied through \( V_{\text{dd}} \). With properly designed test structures, the resolution limit of CBCM is determined by the matching of the two pseudoinverters. Mismatch in the parasitic device capacitances (i.e., \( C_{\text{overlap}} \) and \( C_{\text{junction}} \)) will lead to a small amount of error in the measurement. By designing the pseudoinverters to be small and close together in the test chip, this error can be significantly reduced. This limit has been estimated to be approximately 0.01 fF. To demonstrate this high degree of resolution, a small interlayer capacitance was measured and verified through a robust extraction scheme to be 0.44 fF [3]. The results of this measurement are shown in Fig. 2, where both \( f \) and \( V_{\text{dd}} \) in (2) are varied and the slopes of the lines are proportional to the capacitance being characterized. RMS error of less than 0.5% is achieved using this extraction methodology.
III. METAL-TO-SUBSTRATE CAPACITANCES

The first, and simplest, structure to characterize is that of an isolated metal line over the silicon substrate. By varying the width of a line with a constant length, a linear capacitance versus linewidth plot results, from which area and fringing components of the capacitance can be found. Fig. 3 shows metal 2 capacitance to substrate as a function of drawn width for both measurement and simulation. It can be seen that the intercepts of the two lines are essentially identical, while the slopes are different. The slope in this figure corresponds to the area component of the capacitance to substrate. CBCM yields 19.6 aF/μm for $C_{\text{area}}$, while RAPHAEL gives 15.5 aF/μm. Data on 32 fabrication lots for this process is provided by the manufacturer, giving an average $C_{\text{area}}$ of 20.4 aF/μm$^2$, with values ranging from 11 to 27 [5]. Error bars in Fig. 3 allow for process variation in both the width of the line and the interlevel dielectric (ILD) thickness according to process specifications. The first possible explanation for differences between CBCM and simulation may result in this case from substrate effects that are not taken into account in the simulator. RAPHAEL incorporates a metal ground plane, rather than a doped substrate, in its calculations. Metal-oxide-silicon capacitance has slightly different characteristics than metal-oxide-metal does. Small changes in capacitance could result due to inversion in the field regions or other substrate effects. This is an inherent advantage of measurement in the case of metal-to-substrate capacitances. The varying conductivity of the substrate with frequency is also easily handled with CBCM: measurements can be taken at different frequencies, allowing for different results. In this case, low frequencies are used at which silicon acts as a conductor so no frequency-dependence is seen in Fig. 3. Also, the interconnect structures used in these measurements were fairly long (L = 135 μm) compared to their width. A long, thin metal line will have a much larger fringing component of capacitance than area component. This fact makes the measurements particularly sensitive to $C_{\text{area}}$. In the future, structures of this type should be designed with roughly similar areas and perimeters to avoid potential error [6].

IV. INTERWIRE CAPACITANCES

Capacitance between metal lines of the same layer is referred to as interwire or coupling capacitance. As mentioned earlier, this is a major problem in current and future technologies due to tighter pitch and higher metal aspect ratios. The undesired voltage spikes resulting from this capacitive coupling between lines is commonly referred to as crosstalk. The presence of another nearby line will increase the total capacitance of an isolated line, which was discussed in the previous section. This added capacitance must be taken into account when routing global signals such as clocks, determining driver sizes and line widths/spacings, etc.

In this test chip, our interwire structures were designed to measure this additional capacitance brought on by the presence
of a neighboring wire. Fig. 4 shows our methodology in extracting interwire capacitance. Fig. 5 presents measurement and simulation data for four different spacings of metal 2 wires. The error bars in Fig. 5 allow for process variation that arises due to changes in the width and thickness of the lines (critical dimensions, or CD variation). The maximum added capacitance is around 2 fF per 135 \( \mu \text{m} \) length. The general trend for both CBCM and RAPHAEL is an approximate \( 1/d^2 \) relationship, where \( d \) is the distance between lines. Using a small set of CBCM structures, a simple analytical fit could be made for \( C_{\text{interwire}} \). Implementing this expression in a layout extraction program, very accurate capacitance values for long parallel lines could be calculated.

The minimum spacing of second level metal used in our test chip was 2 \( \mu \text{m} \). In current 0.35-\( \mu \text{m} \) technologies, minimum spacing between second level metal is normally 0.5 \( \mu \text{m} \). Thus, the added capacitance of about 2 fF/135 \( \mu \text{m} \) in our case will be significantly larger. For higher metal layers, interwire effects are more pronounced due to increased metal heights and lessened substrate effects. Since most signals are routed on lower levels, crosstalk does not become critical in higher layers normally carrying power and ground. An additional layout method of reducing crosstalk is to include upper and/or lower ground planes surrounding the signals of interest. In the case of parallel metal 1 lines, a grounded metal 2 plate above the two lines would divert field lines to the ground plane rather than the neighboring signal. A tradeoff is made here, as total capacitance on each line is increased using this technique. CBCM can also be used to accurately measure crosstalk, or \( C_{12} \) in Fig. 4. This involves utilizing several test structures to decouple the vertical and horizontal capacitance components from the total capacitance. From simulation results, \( C_{12} \) can be expected to be two to four times larger than \( C_{\text{interwire}} \).

V. INTERLAYER CAPACITANCES

Interlayer capacitances are significant, especially in the case of wide lines or long, dense arrays. An assumption made in many analytical interconnect models to provide simplicity is that an array of lines behaves as a continuous plate when dealing with interlayer capacitances [7]. We tested this assumption by placing metal 1 lines increasingly closer together underneath a metal 2 plate. We then measured the capacitance on the metal 2 plate. Each overlap was 1.5 \( \mu \text{m} \times 2 \mu \text{m} \), and spacings between metal one lines were 1.5 \( \mu \text{m} \), 3 \( \mu \text{m} \), and 4.5 \( \mu \text{m} \). We found a saturating effect where capacitance was only increased by a few percent when decreasing spacing from 3 to 1.5 \( \mu \text{m} \). Fig. 6 shows our data compared to RAPHAEL simulations. Simulations show a similar saturating effect, although it takes place more gradually, or equivalently, at smaller spacings.

Interlayer capacitances, more than previous structures, bring into focus one major problem in relying solely on interconnect simulations; it is difficult to generate exact input files due to the variance of ILD thicknesses. Without taking scanning electron microscope (SEM) measurements of each structure, it is impossible to simulate interlayer capacitances with complete accuracy. In this case, for example, as metal 1 lines become denser, ILD thickness between first and second level metals is known to become thicker as a result of processing conditions. While the ILD is thickest when spacing is minimum (1.5 \( \mu \text{m} \)), it will be somewhat thinner in the case of 3 and 4.5 \( \mu \text{m} \) spacing. In this analysis, an ILD thickness corresponding to
dense metal 1 was used. This results in the slight undershoot by RAPHAEL at 18 and 24 lines. By varying the ILD thickness within given process specifications (typically 20% or more of variation), a range of capacitances can be determined and are seen from the error bars in Fig. 6 to result in better agreement with CBCM. CBCM implicitly takes any ILD variation into account since it is based on measurement data. As a result of using our technique, we conclude that a metal density of 33% or greater (spacing = 2 width) can be approximated as a plate with negligible loss of accuracy. A subsequent study [8] using a different three-dimensional (3-D) capacitance simulator has corroborated this result.

VI. INTERCONNECT SIMULATION

The interconnect simulator used in this paper employs the finite difference method to compute capacitances. As with most numerical techniques, finite difference generates a mesh to perform its calculations. By using a larger mesh, more accurate results can be obtained at the expense of longer simulation run-times. This point is highlighted in Fig. 7, which demonstrates this accuracy/run-time tradeoff for a metal 2 interwire case, as examined in Section IV. The conclusions drawn from this figure are generally applicable to other interconnect geometries, making a discussion worthwhile. The figure demonstrates that even at $10^5$ grid points, the capacitance values, both $C_{\text{total}}$ and $C_{\text{coupling}}$, have not yet converged to a final value. Also, the run-time can be seen to increase quadratically which implies that there may be an optimum point where any additional accuracy will have to be sacrificed to save time. This optimal point may be different for varied interconnect geometries, making the batch simulation of large sets of structures rather difficult. In addition, 3-D structures with large numbers of conductors, such as data busses, will experience long run-times due to an $N^2$ dependency on conductors in many simulators. For the simulation of Fig. 7, the input file was very simple and consisted only of two conductors and a ground plane. Attempting to simulate a large interconnect structure would result in run-times that are orders of magnitude larger than those shown in this example. It should also be noted that with an increasing number of grid points in Fig. 7, the value of $C_{\text{coupling}}$ is converging toward the value found by CBCM.

It should be emphasized here that measurement is not a replacement for simulation, but a complement. For instance, in early stages of process development, actual silicon may not be available, making CBCM infeasible. At this point in time, simulation can provide good estimates of expected capacitance parameters. Later on, however, actual measurements using CBCM will provide more reliable and accurate data to incorporate into CAD programs and circuit simulations.

VII. CONCLUSIONS

This paper demonstrates the accuracy of the recently introduced CBCM method of characterizing interconnect structures. In future technologies, the number of metal levels will increase beyond six, lower levels will be globally nonplanar due to larger die sizes, and new low-$k$ dielectrics will be introduced which will have anisotropic dielectric constants. All these factors will make CBCM an indispensable tool for interconnect characterization. Important trends in interwire capacitance and saturation effects in interlayer geometries that were previously simulated using a 3-D simulator are verified by CBCM. Furthermore, a discussion of computer simulation for characterizing interconnect pointed out that the use of simulation at the developmental stages of a process might be necessary due to the lack of available test structures. The use of CBCM at later stages, such as process refinement and characterization, demonstrates the complementary nature of measurement and simulation. Other advantages of our new method include the extremely small size of the test structure,
the ease of measurement setup, and a resolution limit around 0.01 fF.

Some important potential applications are shown in Fig. 8: verification of TCAD simulators for specific processes and implementation of accurate measurement data into rules-based capacitance extraction programs. In addition, the monitoring of process variations in a scribe line is another possible application due to the small size of CBCM. Work is underway to use CBCM in providing circuit designers with more accurate technology files for layout extraction, yielding more realistic simulation results.

REFERENCES


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