Epic Platform Integration Guide

Prabal Dutta
Computer Science Division
University of California, Berkeley
Berkeley, California 94720
prabal@cs.berkeley.edu

1 Introduction

This document describes how the Epic Core can be integrated into a new mote platform. Integration has both electrical and mechanical aspects to it that we present (or will someday present) in this document. Note: this document is a work in progress so it will grow as user requirements demand.

2 Electrical Signals

Creating a new mote design based on the Epic Core can require various degrees of integration. The minimum recommended level of electrical integration is shown in Figure 1 and described below. The basic requirements include connecting ground and power supply lines, providing a way to program the Epic, configuring the default state of the external flash memory write protect line, and optionally connecting LEDs to provide visual output. Finally, a variety of I/O lines including SPI, I2C, ONEWIRE, UART, ADC, GPIO, JTAG, RF, and test lines can be exposed for additional functionality.

2.1 Power Supply

GND1, GND2, GND3. The GND1(1), GND2(35), and GND3(52) lines are the digital supply grounds and they are connected together on the Epic Core. Although these three lines are internally connected, they individually provide the preferential ground return for the microcontroller, flash, and radio, respectively.

AGND. The AGND(18) line is the ground return for the analog section of the microcontroller. The AGND signal may be connected to the GND1, GND2, and GND3 lines, but care should be taken to minimize coupling between AGND and the digital ground lines.

DVDD. The DVDD(68) line is the positive voltage supply for the digital circuitry on the microcontroller. The input voltage range for this signal is 1.8 V to 3.6 V. If the DVDD, RVDD, and FVDD voltages are different, then the pairwise difference between any pairs **must not** exceed 300 mV.

RVDD. The RVDD(51) line is the positive voltage supply for the radio. The input voltage range for this signal is 2.1 V to 3.6 V. If the DVDD, RVDD, and FVDD voltages are different, then the pairwise difference between any pairs **must not** exceed 300 mV.

FVDD. The FVDD(34) is the positive voltage supply for the flash memory. The input voltage range for this signal is 2.5 V to 3.6 V. If the DVDD, RVDD, and FVDD voltages are different, then the pairwise difference between any pairs **must not** exceed 300 mV.

AVDD. The AVDD(17) is the positive voltage supply for the analog section of the microcontroller. The AVDD signal may be connected to the DVDD signal but if these signals are connected, a pi-type filter (C1, L1, C2) is highly recommended for reducing the effect of supply noise on the analog segment. Care should be taken to follow the power distribution topology shown in the recommended design. In particular, if power supply connection is J1, the DVDD(68), RVDD(51), and FVDD(34) should fan out from J1 along separate traces, and the AVDD(17) pi filter should be placed close to the AVDD(17) line on the Epic Core.

2.2 Programming

If Epic is to programmed in-system, then a handful of Epic lines must be exposed as well. In particular, programming the system requires DVDD(68), GND(1), TX1(61), RX1(62), TCK(15), and RST#(16) be exposed. The recommended programming port pinout is shown in J2. The suggested programming port is a 2 mm, 2x3, header.

2.3 Reset

The Epic Core can be reset by asserting the RST#(16) line low. It is often convenient to be able to reset a device using a pushbutton. A circuit that provides the suggested debouncing includes S1 (a normally open switch), R4, and C3.

2.4 Flash Write Protect

The Epic Core includes and Atmel AT45DB161D flash memory. This device includes a write protect line that prevents accidental programming of certain sectors. The FLASH_WP#(37) line must be asserted low to enable write-protect and asserted (or pulled) high to disable write protect. The challenge lies in deciding under

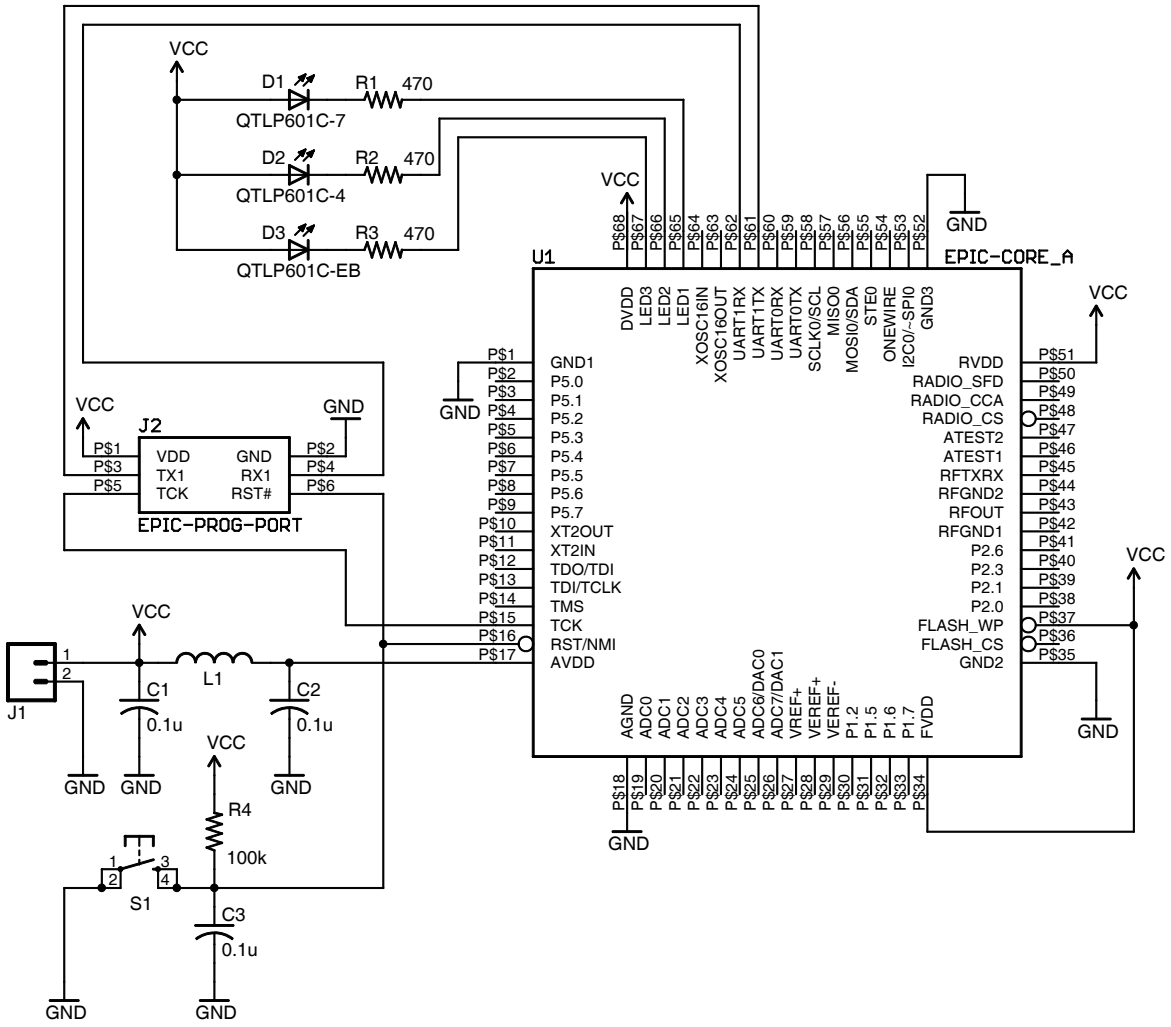

Figure 1. Recommended circuit for a basic mote based on the Epic Core.

what circumstances to protect the flash. If write protection is not used, then this line should be pulled high or connected to FVDD(17) as shown in the recommended circuit.

2.5 LEDs

TinyOS platforms have a history of providing LEDs to indicate status to developers and users. The default TinyOS Epic Core target has allocated three GPIO lines for this purpose: LED1(65), LED2(66), and LED3(67). These three lines are driven low when the LED is turned on using the TinyOS 2.0 API calls `Leds.led0On`, `Leds.led1On`, and `Leds.led2On`, respectively. Therefore, the recommended circuit for driving the LEDs is to connect the anode of the LED to VCC and the cathode through a series current limiting resistor to the LED1, LED2, and LED3 lines as shown in the recommended circuit.

3 Libraries

A number of useful schematic symbols, land patterns, and device footprints are available in Eagle CAD format. The filename is `berkeley-epic.lbr` and this library is available online at Epic download website. The `berkeley-epic.lbr` contains a variety of parts but the following are most relevant for integrating the Epic Core into a new mote design.

- **EPIC-CORE_A.** The Epic Core symbol (rev A) that can be added to the schematic for a new mote design. The land pattern (or footprint) for the Epic Core is EPIC-LCC68.
- **EPIC-PROG-PORT.** The recommended programming port for the Epic Core. The land pattern (or footprint) for the programming port is HEADER2x3x2mm.