Chaos shift keying communications system using self-synchronising Chua oscillators

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Indexing terms: Chaos, Chua's circuit, Communications and signal processing

The laboratory test results of a modified Chua oscillator are presented. The intent is to show some of the performance limitations when attempting to obtain a chaotic receiver to a similar transmitter. Amplitude variations and multiple carriers in the same channel are shown to have significant effects.

Introduction: There is considerable interest in the possibility of using synchronised chaotic circuits in communication systems. In one system, called 'chaos shift keying' (CSK) [1] the parameters of a Chua oscillator are controlled and one of its state variables is transmitted to a set of two or more stable subcircuits that can individually detect the presence of a particular attractor. Each attractor corresponds to a specific data symbol. We present some practical methods for implementing and measuring the performance of a CSK system. We also present results from laboratory tests of prototype hardware.

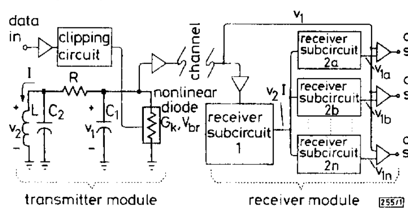

Fig. 1 *Block diagram of experimental setup*

Apparatus: Fig. 1 shows the block diagram of our experimental CSK system. The state equations governing the behaviour of the Chua oscillator [2] are

$$\left.\begin{aligned}\frac{dI}{dt} &= -\frac{1}{L}V_2\\ \frac{dV_2}{dt} &= \frac{1}{C_2}I_3 - \frac{G}{C_2}(V_2 - V_1)\\ \frac{dV_1}{dt} &= \frac{G}{C_1}V_2 - \frac{G_k}{C_1}V_1 - K\end{aligned}\right\} \quad (1)$$

where L, C_2, C_1, and G (= $1/R$) are circuit parameters.

The constant K is determined by the characteristics of the nonlinear diode and is shown in eqn. 2:

$$K = \begin{cases} V_{br}(G_b - G_a) \\ 0 \\ V_{br}(G_a - G_b) \end{cases}$$
$$\text{and } G_k = \begin{cases} G + G_b & \text{if } V_1 < -V_{br} \\ G + G_a & \text{if } -V_{br} < V_1 < V_{br} \\ G + G_b & \text{if } V_1 > V_{br} \end{cases} \quad (2)$$

where G_a and G_b are the slopes of the diode, and V_{br} is its breakpoint voltage.

It has been suggested [1] that the transmitter attractor can be varied by switching an additional conductance in parallel with the diode. We have chosen to change only K, which will alter the fixed points and nonlinear breakpoints of the transmitter while keeping the Lyapunov exponents constant. K is easily changed using a clipping circuit that alters V_{br}. This allows different transmitter states to retain much of their original dynamic behaviour while still operating on different attractors.

Receiver block: The first receiver subcircuit (Fig. 1) uses the transmitted signal V_1 to create replicas of the other two system state variables I' and V_2'. The second receiver subcircuit uses I' and V_2', to generate V_1'. V_1' is compared to V_1 and an error signal is produced which is used to determine when the system is locked-in. Varying the reference can set the extent of the parameter space over which lock-in is obtained, and hence vary the system sensitivity.

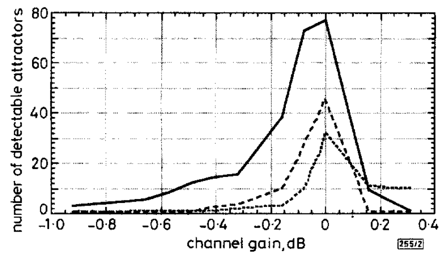

Fig. 2 *Data thoughtput against channel gain*

——— G = 535μS
–·–·– G = 533μS
····· G = 526μS

Amplitude sensitivity: Amplitude sensitivity was measured by changing the gain of the channel (from a nominal 0dB) and noting the effect on the number of detectable attractors (symbols in our context). Fig. 2 shows that CSK is quite sensitive to changes in the channel gain. For the most robust parameter set (G = 526μS), amplitude variations as small as 0.2dB caused large changes in the system performance.

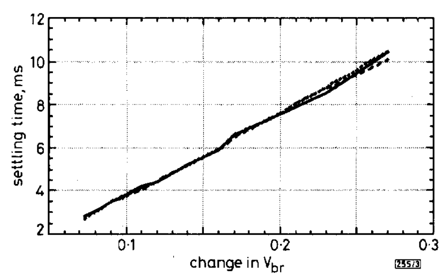

Fig. 3 *Settling time against attractor separation*

——— G = 535μS
– – – – G = 533μS
- - - - - G = 526μS

Settling and unsettling times: We measured the relationship between settling time and system throughput. This is directly related to the 'separation' in the parameter space between locked and unlocked attractors and is a function of K, which depends on V_{br} (Fig. 3). A similar response for unsettling times was observed.

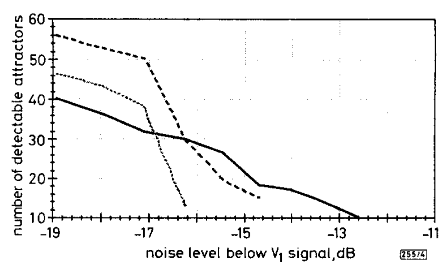

Fig. 4 *S/N performance*

——— G = 535μS
- - - - - G = 533μS
– – – – G = 526μS

SNR and SIR measurements: To test the SNR characteristics of CSK, a flat noise source was generated, mixed with V_1 and fed into the first receiver subsystem. The number of detectable attractors was measured and the results are shown in Fig. 4.

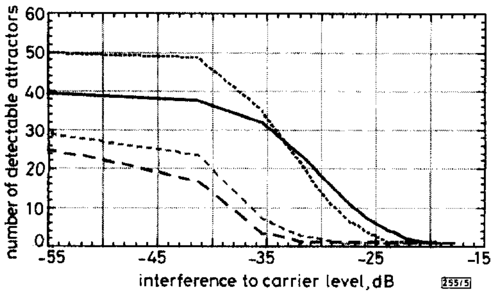

Fig. 5 *Sensitivity to interfering carriers*

——— F_c = 1kHz
– – – – F_c = 3kHz
— — F_c = 4kHz
- - - - - F_c = 6kHz

Fig. 5 shows the interfering signal level against attractors for G = 526µS. We calculated the eigenfrequency to be ~3.7kHz and it can be seen that interfering signals near this frequency cause a dramatic drop in the number of detectable states. Signals offset by > ~1.8kHz appear to have much less effect on system performance. This indicates that two similar chaotic signals that overlap in the same channel would interfere with each other to a significant extent.

Conclusions: We have demonstrated methods that can be used to measure the performance of a CSK communication system. Data have been presented that show SNR and SIR performance. The sensitivity of the system is limited by interfering carriers close to the eigenfrequency. In addition, significant sensitivity-to-channel gain variations are observed.

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Realisation of *n*th-order voltage transfer function using CCII+

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Indexing terms: Current conveyors, Network synthesis

A method for realising voltage transfer functions using only plus-type current conveyors is presented, and a circuit that realises the general *n*th-order transfer function is given. This circuit is suitable for integration and the use of only plus-type current conveyors (CCII+) simplifies the configuration.

Introduction: The realisation of voltage transfer functions using current conveyors (CCIIs) as active elements has received much attention in the literature [1 – 6]. In this work, a synthesis procedure for generating CCII+ active filters is presented. The proposed method is based on drawing the signal flow graph directly from the given transfer function and then obtaining the active circuit from the graph. We present a general *n*th-order current conveyor circuit for which the element values are expressed in terms of *n*th-order voltage transfer function coefficients. Furthermore, the use of only plus-type current conveyors simplifies the configuration.

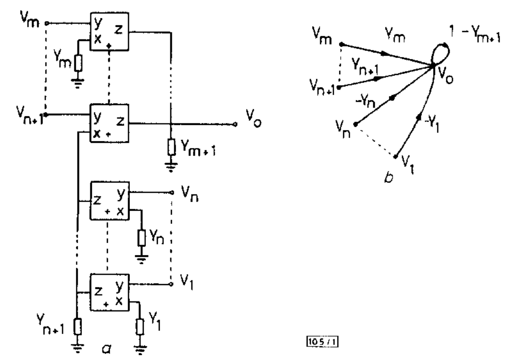

Fig. 1 *CCII+ substrate network and associated signal flow graph*

a CCII+ subnetwork
b Associated signal flow graph

Synthesis procedure: Consider the subnetwork shown in Fig. 1*a*. Using the defining equations

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix} \qquad (1)$$

for the plus-type second generation current conveyor [7], it can be shown that the signal flow graph in Fig. 1*b* corresponds to the subnetwork in Fig. 1*a*.

If a given transfer function is represented by a suitable signal-flow graph in such a way that each node (except the input node) has a self-loop-gain equal to the difference between unity and any RC admittance function, and each branch has a transmittance equal to any ±RC admittance function, then the corresponding circuit realisation can be easily found using Fig. 1.

Let the general *n*th-order voltage transfer function be given by

$$\frac{V_o}{V_i} = \frac{a_n s^n + a_{n-1} s^{n-1} + ... + a_1 s + a_0}{s^n + b_{n-1} s^{n-1} + ... + b_1 s + b_0} \qquad (2)$$

This transfer function can be represented by a signal flow graph, as shown in Fig. 2*a*, which is suitable for the realisation procedure. Then the CCII+ circuit in Fig. 2*b* can be easily obtained with the aid of Fig. 1. This circuit uses grounded capacitors, which are desirable from the integrated circuit implementation point of view. It should be noted that this circuit contains at most $3n$–2 current conveyors (all of them are plus-type), n+1 capacitors (n of them being equal), $3n$–1 resistors (n–1 of them being equal). Furthermore, if the voltage transfer function of the general circuit in Fig. 2*b* is calculated, the denominator is

$$\begin{aligned}&(C_1 C_2 ... C_{n-1} C_n) s^n + (G_{2n} C_1 C_2 ... C_{n-1}) s^{n-1} + ... \\ &+ (G_4 ... G_{2n-1} C_1) s + (G_2 G_3 ... G_{2n-1})\end{aligned} \qquad (3)$$

Since no difference terms are involved, the circuit is expected to have low sensitivity characteristics.

If the proposed procedure is applied to the biquadratic voltage transfer function, the obtained circuit is similar to the circuits in [5]. However, calculation of the element values is straightforward and does not require matching of the coefficients of the transfer function with the element parameters. Furthermore, higher-order filters can be realised with this method.