Advanced Analog Integrated Circuits

Operational Transconductance Amplifier III

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Telescopic OTA
Output Swing versus Gain

\[ G = \frac{v_o}{v_i} \]

\[ a_{vo} = \frac{dv_o}{dv_i} \]
Cascoded Telescopic OTA
Realizing $V_{bias}$
Input Capacitance
Neutralization Capacitor Layout

- $C_n$
- Note that this layout also minimizes wiring $C_{gd}$
- For high-speed applications

Ref: Z. Deng, 12/2011
Improved Swing: Folded Cascode
Folded Cascode Noise
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Slewing

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Differential Pair Transconductance

- Nonlinear:
  - for $V_{id} > V^*$, $G_m \ll g_{m1}$
Initial Transient

- Differential mode half circuit:
Initial Transient

\[
V_{id,step} \quad V_{od,step} \quad V_{od,slew} \quad V_{od,lin} \quad V_{xd,step} \quad V_{xd,lin} \quad V_{id} \quad V_{xd} \quad V^* \quad 0 \quad t_{slew} \quad t_{lin} \quad t_s \quad V_{od}=cV_{id}
\]
Circuit Model During Slewing

\[ V^* \]
Linear Settling
Settling Time with Slewing

\[ t_s = t_{slew} + t_{lin} = t_{slew} + \frac{V_{id,step}}{C_s} \left( \frac{C_s + C_x + (C_f || C_L)}{V_{xd,step}} \right) \left( \frac{C_s}{C_s + C_x + (C_f || C_L)} \right) - V^* - \tau \cdot \ln \left( \varepsilon_d \frac{cV_{id}}{V_{od,lin}} \right) \]

- Note that for \( V_{xd,step} < V^* \) the circuit won’t slew at all
For circuits with significant slewing (large input compared to $V^*$, small closed-loop gain $c$)

1. Start by assuming a slewing time, e.g. 50% of $t_s$
2. Design and verify that linear settling completes within $t_{lin}$ (apply only small steps during simulation to avoid slewing)
3. Now verify with a full-scale input step and check the actual ratio of $t_{slew}/t_{lin}$
4. Iterate until the design and verification match

Typically you get convergence in a few iterations

Slewing is power efficient
- Entire bias current used to charge load
- But limits maximum speed
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Two Stage OTA

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Miller Compensated 2-Stage OTA
Process Insensitive Realization of $R_z$
Slewing in 2-Stage Miller OTA

Asymmetric Slewing
Why is Symmetric Slewing Important?
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OTA Design Flow

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Divide and Conquer Design Flow

• Determine suitable topology based on specifications, e.g.
  – Single or multi-stage
  – Gain boosting

• Script based design
  – Step 1: small-signal
    • Make reasonable assumptions (output range, \( L, \alpha \) etc.)
    • Ignore slewing
  – Step 2: large-signal
    • Compute slewing time (use ideal CMFB, biasing), re-optimize
    • Add CMFB, verify stability and settling
      – At this point your design should meet the settling and dynamic range requirements
    • Add biasing, check static settling accuracy
    • Proceed to layout phase: # fingers for transistors, …
Remedies (Examples)

• What to do when the design does not meet the specifications?
  – Typically the case due to assumptions that are not met

• Examples:
  1. Unity-gain bandwidth falls short of design target
     • Typical cause: self-loading (e.g. $C_{DB}$)
     • Solution: decrease $C_L$
  2. Excessive noise
     • Typical cause: not all noise sources considered in design, e.g. noise from cascodes (verify!)
     • Solution: Scale all capacitors, bias currents, and channel width by
       $\left(\frac{V_{n\text{-target}}}{V_n}\right)^2$

• Other shortcomings require more significant modification
  – Insufficient phase margin: increase cascode $f_T$?
  – Insufficient low frequency gain: increase $L$, add boosters, multi-stage
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OTA Examples

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High Gain

[Bult, JSSC 1992]
Differential Boosters

[Ahmadi, TCAS-II, 2006]
Boosted Boosters

[Chiu, JSSC 2004]
2-Stage OTA with 2 CMFB Loops

[Yang, JSSC 2001]
2-Stage OTA with Ribner Compensation

[Abdighted, JSSC 1999]
Simpler?

pseudo-differential

[Nauta OTA, Irfansyah, 2014]
Differential & Low Power

[Groenen, ISSCC 2016]