Advanced Analog Integrated Circuits

Switched Capacitor Gain Stages

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OpAmp versus OTA

OpAmp

OTA

\[ \equiv \]
Gain Stages

Resistive Feedback

Capacitive Feedback
Low Frequency Gain

Resistive Load

![Resistive Load Circuit](image)

Capacitive Load

![Capacitive Load Circuit](image)
### Transconductor Choices

<table>
<thead>
<tr>
<th>BJT</th>
<th>MOS</th>
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\[ \beta = 100, \ V^* = 150\text{mV} \]
Aside: MOS Voltage Buffers
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Switched Capacitor Gain Stage

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SC Gain Stage

Switches controlled from non-overlapping 2-phase clock:

Note: *important* details of clocks and switches will be discussed later.
Multiphase Clock Generators

Cross-coupled RS flip-flop

Delay sets nonoverlap period. (time period in which both $\phi_1$ and $\phi_2$ are 0).

Spectre:

```
phil (vphil 0) vsourcetype=pulsevalu0=0valu1=1.8 +period=1/fswidth=0.45/fsdelay=0.01/fs
```
Phase 1

![Diagram of a phase 1 SC (Switched Capacitor) gain stage circuit with capacitors $C_1$ and $C_2$, switches $\phi_1$, $\phi_2$, $\phi_{1e}$, and $\phi_{2b}$, and input $v_i$ and output $v_o$.]}
Phase 2
Charge Conservation
Transient Analysis
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Time Invariant Circuits

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Switched Capacitor Circuits
Time Invariant and Linear
Periodic ac Simulation (Spectre)

• Perform first a “periodic operating point analysis”:

  pss1 pss fund=fs maxacfreq=20*fs
  +errpreset=conservative harmonicbalance=no
  – fund is the sampling frequency
  – maxacfreq is the highest frequency from which folding noise is relevant. Run several circuit simulations, doubling the value each time until the result no longer changes.

• Now perform the ac analysis:

  pac1 pac start=1k stop=10G log=100
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Sampling Noise

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Sampling Noise

Noise in phase 1 (sampling phase):

Voltage across $C_1$:

RC Noise Spectrum

\[ S_y(f) = \frac{k_B T_r}{C f_s} \frac{2}{1 + e^{-2a} \left(1 - \cos 2\pi f T\right)} \]

\[ a = \frac{T}{R_{sw} C} = \frac{T}{\tau} \quad \text{and} \quad T = \frac{1}{f_s} \]

\[ \int_0^{f_s/2} S_y(f) df = \frac{k_B T_r}{C} \]

- Noise essentially white for \( T/\tau > 3 \)
- Settling constraints ensure that this condition is usually met in practice, e.g. \( T/\tau > 10 \)
Noise Folding Interpretation

Noise densities:

Continuous time

Discrete time

Ratio:

Effective Noise Bandwidth
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SC Noise Analysis

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Circuit for Noise Analysis
Noise in Phase 1
Equipartition Principle
Noise in Phase 2
Total Integrated Amplifier Noise

\[ R_o \approx \frac{1}{\beta g_m} \]
Total Noise from Phases 1 & 2
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Noise Simulation

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Methods to Simulate Noise for Verification

1. .noise analysis
   - Linear time-invariant circuits only
   - For time variant circuits, simulate each phase separately and combine results manually (as in hand analysis)

2. Periodic noise analysis
   - Analog to pac
   - Perform pss analysis first

3. Transient noise analysis
   - Closest to “reality”, very general
   - Average results from many simulations
   - Good alternative when pss has convergence problems
   - Can be slow …


Periodic Noise Simulation (Spectre)

- Perform first a “periodic operating point analysis”
- Then perform the pnoise analysis:
  
  pnoise1 pnoise (vo 0) fund=fs start=0 stop=fs/2
  +noisetype=timedomain maxsideband=150
  +noisetimepoints=[ 1us ]

  - noisetype=timedomain instructs the simulator to compute the spectrum of discrete time noise samples at specified sampling instances
  - maxsideband=150 sets the maximum frequency relative to fs for which noise folding is significant. Try doubling this value and increase until simulator output converges.
  - noisetimepoints=[ 1us ] is the sampling instance. For the SC gain stage, this is near the end of phase 2
  - See simulator docs and http://www.designers-guide.org/analysis/sc-filters.pdf