EE105 Lecture : MOSFETs

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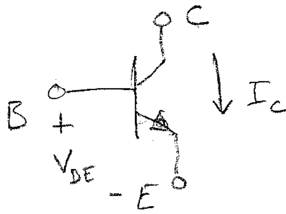
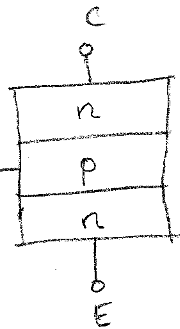
Review BJTs



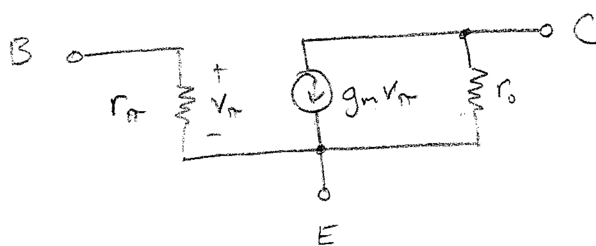
$I_c = I_s e^{V_{BE}/V_T}$

V_T = thermal voltage = $\frac{k_B T}{q_e}$

I_s = saturation current



small signal model



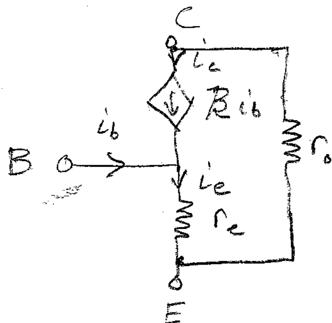
$g_m = \frac{\partial I_c}{\partial V_{BE}} = I_s \frac{V_{BE}}{V_T} e^{V_{BE}/V_T} = \frac{I_c}{V_T}$

$r_o = \frac{V_A}{I_c}$

V_A = Early voltage

$r_\pi = \frac{\beta}{g_m}$

Alternate model (equivalent)



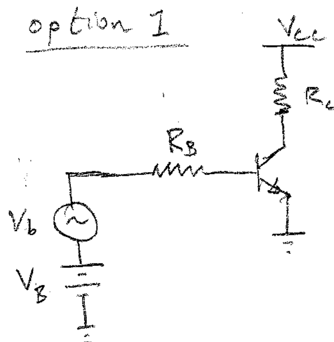
$r_e = \frac{\beta}{\beta + 1} \cdot \frac{1}{g_m} \approx \frac{1}{g_m}$

=> current controlled version

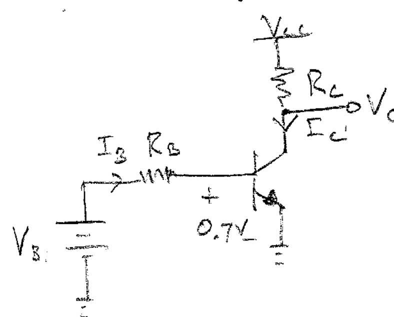
Common emitter amplifier (DC coupled)

Biasing

option I



Large Signal



$I_B = \frac{V_B - 0.7V}{R_B}$

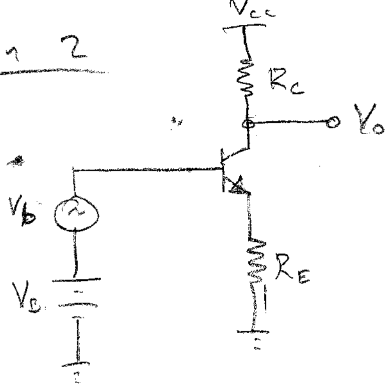
$I_c = \beta I_B$

$V_o = V_{cc} - I_c R_c$

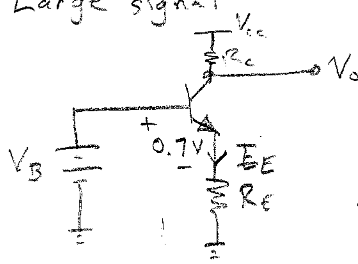
Problems ?

- collector current set by β → may not be a very stable quantity over temp, etc.
- resistive divider between R_B + r_π → attenuates signal

option 2



Large signal



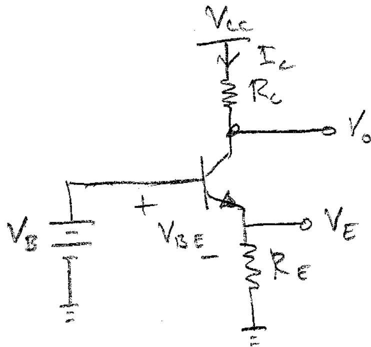
$$I_E = \frac{V_B - 0.7V}{R_E}$$

$$I_c \approx I_E$$

$$V_o = V_{cc} - R_c I_c$$

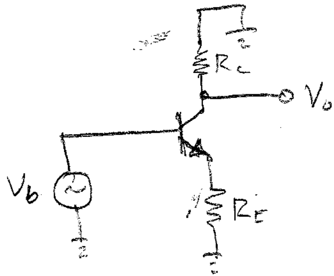
Advantage: I_c independent of β (assuming $\beta >> 1$)
No voltage division at input.

Known as emitter degeneration
-actually a feedback technique

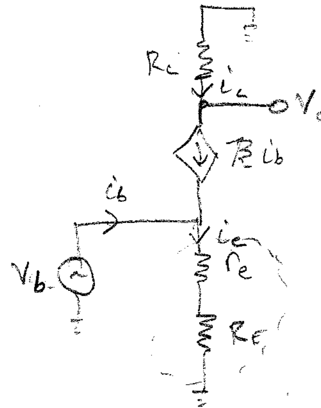


- If $I_c \uparrow \Rightarrow V_E \uparrow \Rightarrow V_{BE} \downarrow \Rightarrow I_c \downarrow$
- ensures stable I_c

Small signal



=>



- r_e & R_E can be lumped together
- $i_e = \frac{V_b}{R_E + r_e}$
- $\beta \to \infty$

  $\Rightarrow i_c = i_e$
- $V_o = -i_c R_c$

  $= -i_e R_c$

$$\boxed{\frac{V_o}{V_b} = -\frac{R_c}{R_E + r_e}}$$

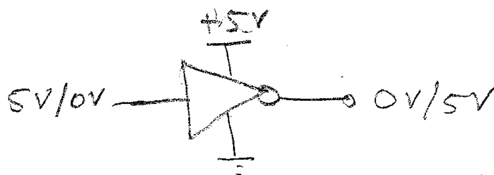
MOSFETs

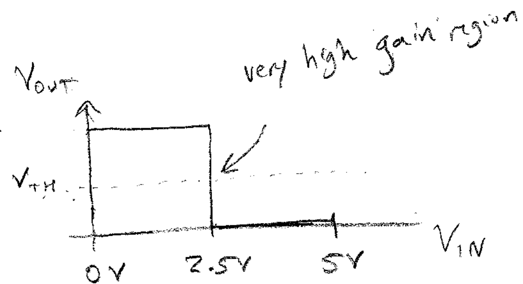
Shortcomings of BJTs

- Finite input resistance
- Require DC base current
- Incompatible with constant voltage base drive schemes (due to p-n junction between BE)

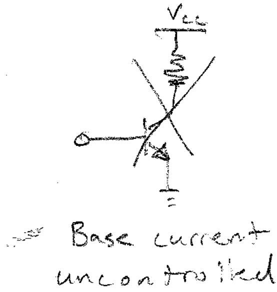
Application: Logic circuits

Inverter

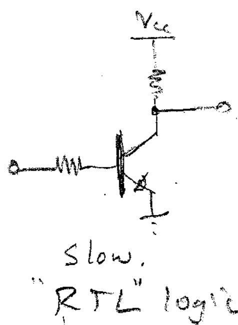




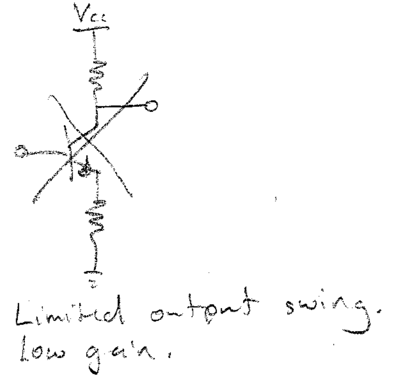
How can we make this with BJTs?



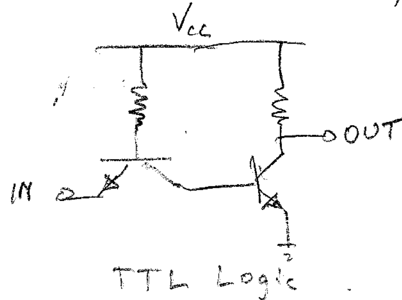
Base current uncontrolled



Slow. "RTL" logic

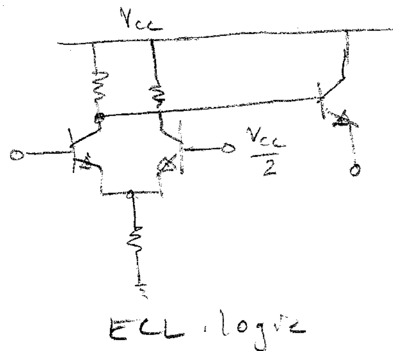


Limited output swing. Low gain.



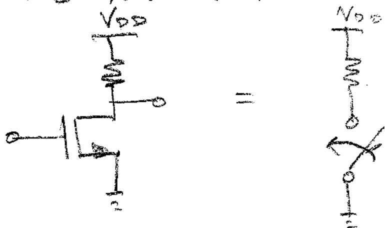
TTL Logic

- All consume static power
- require resistors



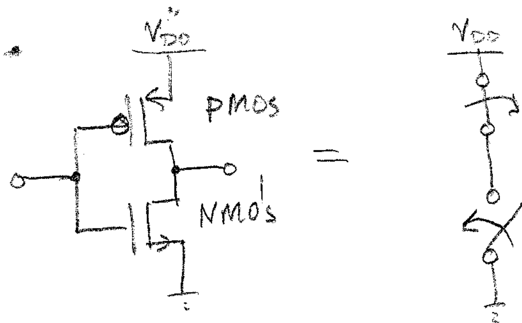
ECL logic

What if we had a true voltage controlled device?



- Input current = 0 (static)
- No current consumption when switch is open
- Input & output levels are compatible.

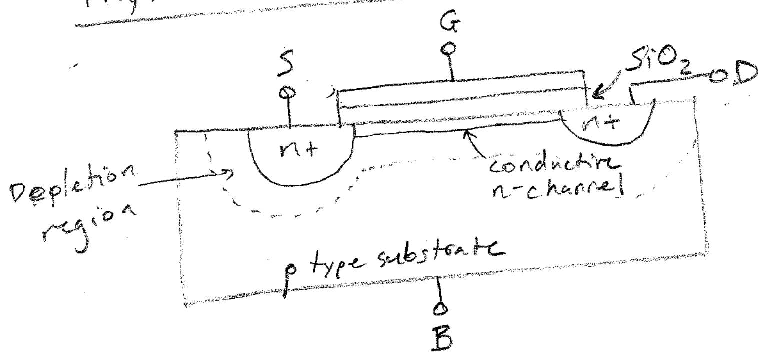
Complementary logic

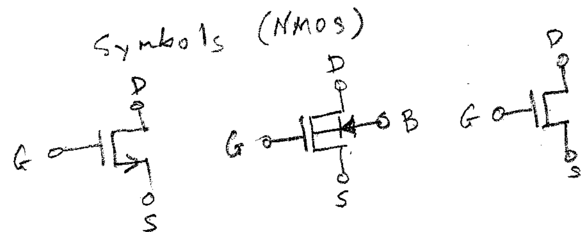


- Switches are never closed simultaneously
- No static power consumption
  - there is still dynamic power consumption associated with charging gate cap. (more later)

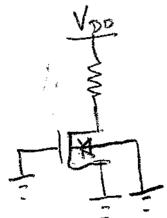
PMOS: on with 0 input
NMOS: on with V_{DD} input

Physical device (NMOS)



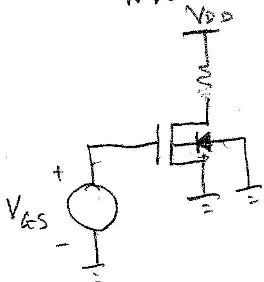


Idea: The conductivity of the channel (region under gate) is modulated by the gate to B/S/D voltage.



⇒ No gate bias, no conductive channel between S & D. D/B form a reversed biased PN junction
∴ there is no drain current.

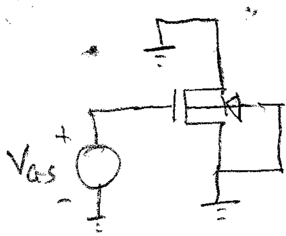
What happens if we apply bias?

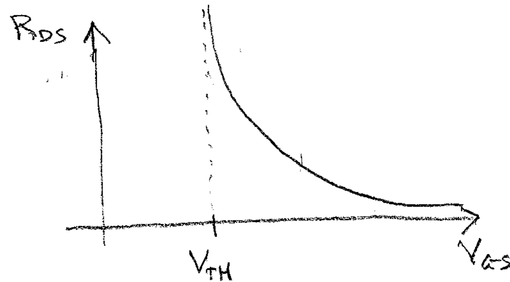


1. Depletion region begins to form under gate. Holes are pushed downward, leaving behind a region of high (negative) space charge.
2. After a critical point, a thin layer of electrons forms right under the gate, enabling current flow. ⇒ known as "inversion"

- critical point = threshold voltage

The FET as a controlled resistor





$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})} \quad (6.12)$$

① μ_n = electron mobility $\left[\frac{cm^2}{Vs}\right]$ Note: v_e = electron drift velocity = $\mu_n E$ (E = electric field)

② C_{ox} = Gate to channel capacitance per unit area $\left[\frac{F}{m^2}\right]$

③ W = device width [m]

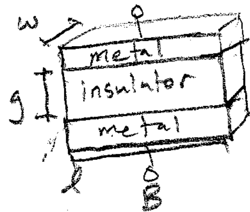
④ L = channel length [m]

⑤ V_{TH} = threshold voltage [V]

① • determined by doping, materials.
• no control by circuit designer

② $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{\text{permittivity of dielectric}}{\text{thickness of gate oxide}}$

Review: parallel plate capacitor



$C = \frac{\varepsilon A}{g}$, $A = wl$

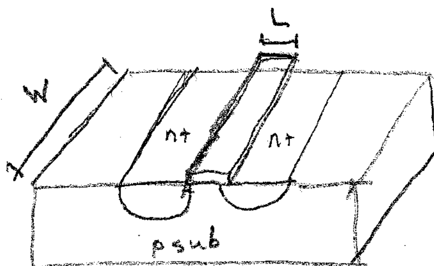
Physics: $D = \varepsilon E$ (Maxwell's equation)

$= \varepsilon \frac{V}{g}$

$Q = DA = \frac{\varepsilon A}{g} V$

$C = \frac{Q}{V} = \frac{\varepsilon A}{g}$

③ + ④

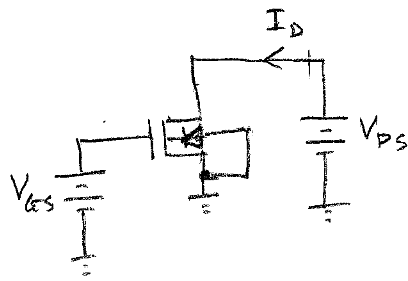


W ↑, L ↓ ⇒ R_{DS} ↓

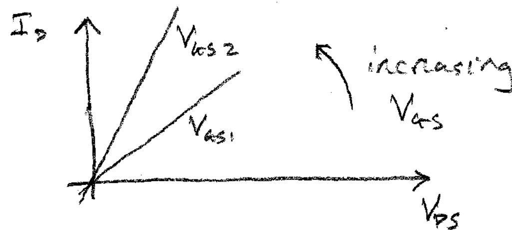
⑤ Roughly twice the Fermi Voltage. controlled by doping.
• No direct ckt. designer control, but typically high + low V_{TH} devices are available.

The FET as a current source. (pinch off effect)

What happens when we apply D to S voltage?

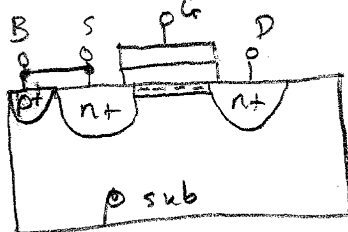


For small V_{DS} => resistive operation

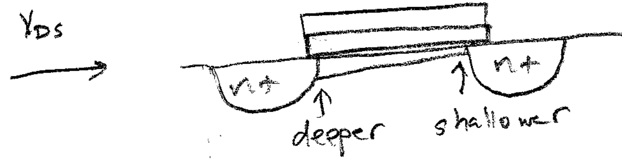


How small?

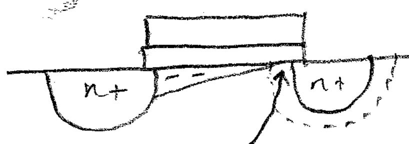
- MOSFETs are symmetric
- We assumed constant channel depth from D to S



V_{DS} →



- When $V_{GD} < V_{TH}$, the channel pinches off



Device still conducts because of very high Electric field in this region.

Rearrange this equation

$V_{GD} < V_{TH}$

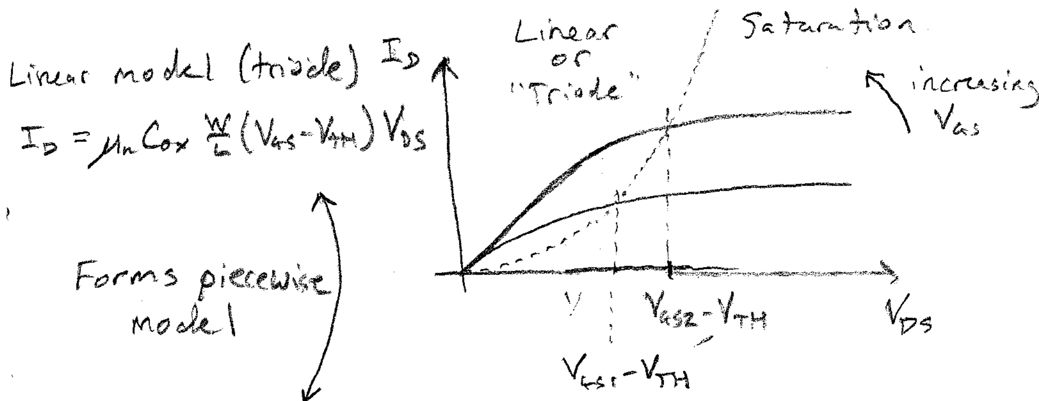
$V_G - V_D < V_{TH}$

$V_D > V_G - V_{TH}$

$V_D - V_S > V_G - V_S - V_{TH}$

"Saturation" condition: $\boxed{V_{DS} > V_{GS} - V_{TH}}$

Linear model (triode) $I_D = \mu_n C_{ox} \frac{W}{L}(V_{GS}-V_{TH})V_{DS}$



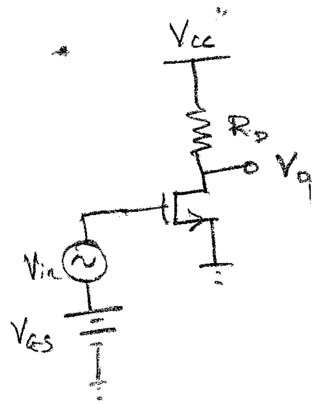
Forms piecewise model

Notes:

- $I_{D,sat}$ still has slight dependence on V_{DS} → ch. length mod. (more later)

Square Law model (saturation): $I_{Dsat} \approx \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS}-V_{TH})^2 \quad (V_{DS} > V_{GS}-V_{TH})$

The MOSFET as an amplifier (common source)



• Assume $V_{DS} > V_{GS} - V_{TH}$ (saturation)

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{GS} + V_{in} - V_{TH})^2$$

$$\frac{\partial I_D}{\partial V_{in}} = \mu_n C_{ox} \frac{W}{L} (V_{GS} + V_{in} - V_{TH})$$

$$V_{in} << V_{GS} - V_{TH} \Rightarrow \frac{\partial I_D}{\partial V_{in}} = \mu_n C_{ox} \frac{W}{L} V_{ov}$$

V_{ov} = overdrive voltage

tells you how "on" the transistor is.

$$g_m = \frac{\partial I_D}{\partial V_{in}} = \text{small signal transconductance}$$

$$V_o = V_{o,DC} + v_o = V_{cc} - I_{Dsat} \cdot R_D - g_m V_{in} \cdot R_D$$

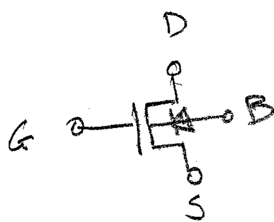
$$\text{Small signal gain} = \frac{\partial v_o}{\partial v_{in}} = -g_m R_D$$

* Linearity is a big assumption.
Always remember where these equations come from,
a Taylor series representation of the large signal model.

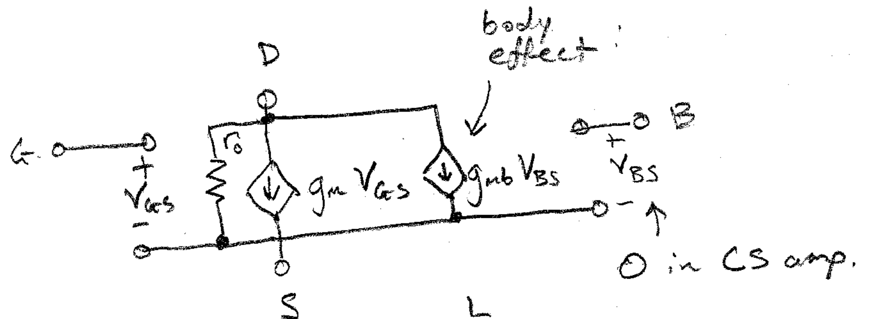
Ex. $I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2$

Calc. Taylor series about $V_{GS} = V_{GS0}$, drop high order terms.

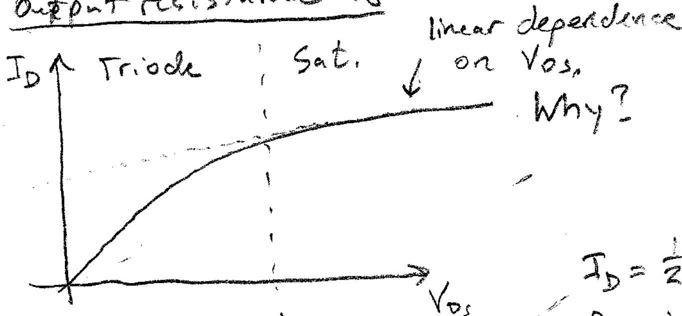
Small signal model (DC)

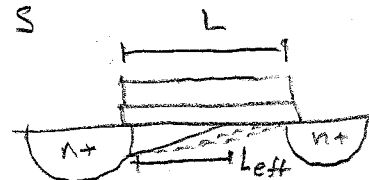


$\Rightarrow$



Output resistance r_o



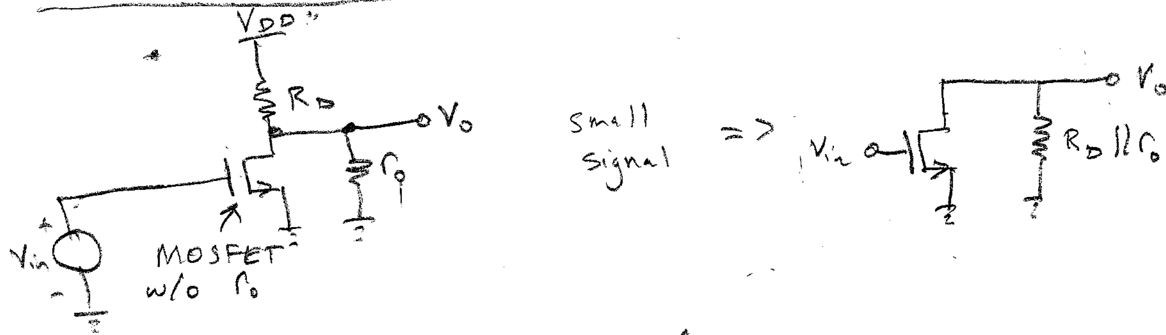


• Depending on V_{DS}, pinch off point will move
• Effectively modulates ch. length

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS})$$

λ = ch. length mod. parameter

Impact of Ch. length mod



- r_o limits voltage gain of FET.
- Let $R_D \to \infty$ => $a \to -g_m r_o$
- High voltage gains useful for
  - minimizing steady state error in op-amp based ctrl. circuits.
  - improving linearity of feedback circuits
  - boosting signal levels for interfacing with ADC, for example.